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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR

NP80N04MHE

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The NP80N04MHE is N-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NIDOONIO AMUEL OAO, AN	Pure Sn(Tin)	Tube	TO-220(MP-25K)
NP80N04MHE-S18-AY		50 p / tube	Тур. 1.9 g

FEATURES

- Channel temperature 175 degree rated
- Super low on-state resistance $R_{DS(on)} = 8.0 \ m\Omega \ MAX. \ (V_{GS} = 10 \ V, \ I_{D} = 40 \ A)$
- Low Ciss: Ciss = 2200 pF TYP.
- Built-in gate protection diode

(TO-220)



ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vgs = 0 V)	VDSS	40	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC) Note1	ID(DC)	±80	Α
Drain Current (Pulse) Note2	D(pulse)	±280	Α
Total Power Dissipation (T _A = 25°C)	Рт	1.8	W
Total Power Dissipation (Tc = 25°C)	Рт	120	W
Channel Temperature	Tch	175	°C
Storage Temperature	Tstg	-55 to +175	°C
Single Avalanche Current Note3	las	52 / 31 / 13	Α
Single Avalanche Energy Note3	Eas	2.7 / 96 / 169	mJ

Notes 1. Calculated constant current according to MAX. allowable channel temperature.

- **2.** PW \leq 10 μ s, Duty cycle \leq 1%
- 3. Starting Tch = 25°C, Rg = 25 Ω , Vgs = 20 \rightarrow 0 V (See Figure 4.)

THERMAL RESISTANCE

Channel to Case Thermal Resistance	Rth(ch-C)	1.25	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	83.3	°C/W

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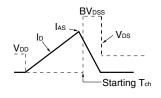


ELECTRICAL CHARACTERISTICS (TA = 25°C)

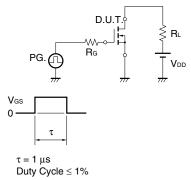
Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Zero Gate Voltage Drain Current	IDSS	Vps = 40 V, Vgs = 0 V			10	μΑ
Gate to Source Leakage Current	Igss	Vgs = ±20 V, Vps = 0 V			±10	μΑ
Gate to Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	2.0	3.0	4.0	٧
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 40 A	15	31		S
Drain to Source On-state Resistance	RDS(on)	Vgs = 10 V, ID = 40 A		6.2	8.0	mΩ
Input Capacitance	Ciss	Vps = 25 V		2200	3300	pF
Output Capacitance	Coss	Vgs = 0 V		490	730	pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		230	410	pF
Turn-on Delay Time	t d(on)	VDD = 20 V, ID = 40 A		24	52	ns
Rise Time	t r	Vgs = 10 V		14	36	ns
Turn-off Delay Time	t _{d(off)}	$R_G = 1 \Omega$		44	88	ns
Fall Time	t f			15	37	ns
Total Gate Charge	Q _G	VDD = 32 V		40	60	nC
Gate to Source Charge	Qgs	Vgs = 10 V		12		nC
Gate to Drain Charge	Q _{GD}	ID = 80 A		16		nC
Body Diode Forward Voltage	V _{F(S-D)}	IF = 80 A, VGS = 0 V		1.0		٧
Reverse Recovery Time	trr	IF = 80 A, Vgs = 0 V		40		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		50		nC

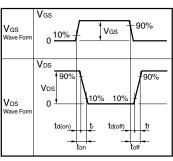
TEST CIRCUIT 1 AVALANCHE CAPABILITY

$\begin{array}{c} \text{D.U.T.} \\ \text{Rg} = 25 \ \Omega \\ \text{VGs} = 20 \rightarrow 0 \ V \end{array} \begin{array}{c} \text{PG.} \\ \text{\downarrow} \\ \text{\downarrow} \\ \text{\downarrow} \end{array} \begin{array}{c} \text{D.U.T.} \\ \text{\downarrow} \\ \text{\downarrow} \\ \text{\downarrow} \end{array} \begin{array}{c} \text{\downarrow} \\ \text$



TEST CIRCUIT 2 SWITCHING TIME





TEST CIRCUIT 3 GATE CHARGE



TYPICAL CHARACTERISTICS (TA = 25°C)

Figure 1. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

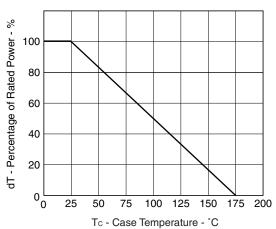


Figure 3. FORWARD BIAS SAFE OPERATING AREA

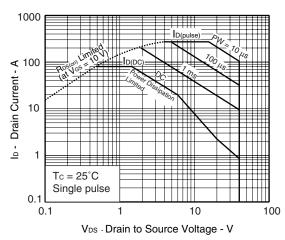


Figure2. TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

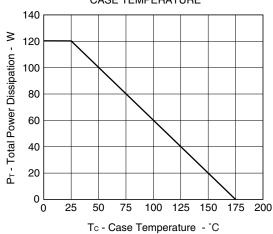


Figure4. SINGLE AVALANCHE ENERGY DERATING FACTOR

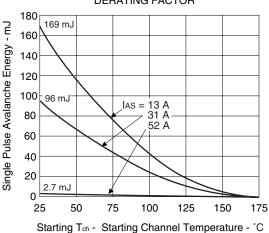
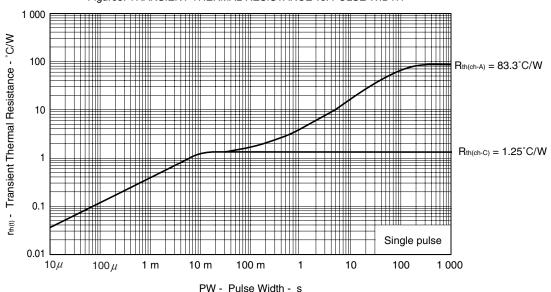


Figure 5. TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



3

Figure 6. FORWARD TRANSFER CHARACTERISTICS

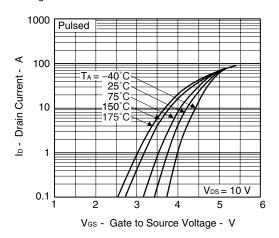


Figure8. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

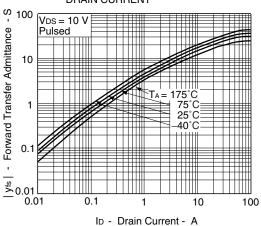


Figure 10. DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

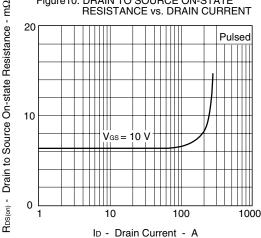
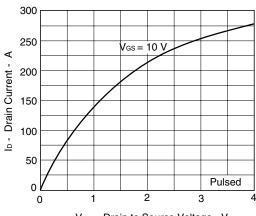


Figure 7. DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



VDS - Drain to Source Voltage - V

Figure9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

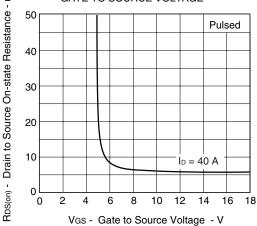
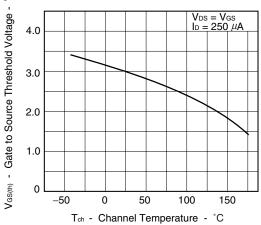


Figure 11. GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE





ШΩ

Figure 12. DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

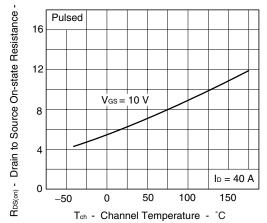


Figure 13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

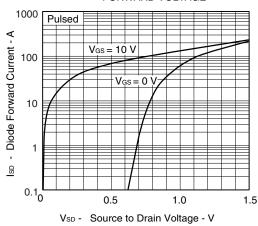


Figure 14. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

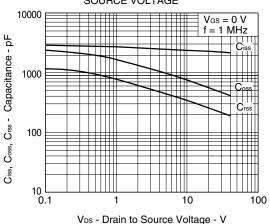


Figure 15. SWITCHING CHARACTERISTICS

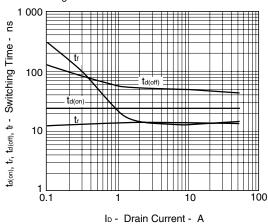


Figure 16. REVERSE RECOVERY TIME vs. DRAIN CURRENT

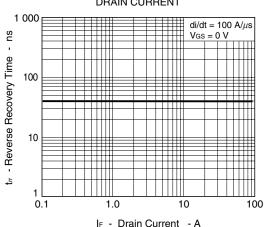
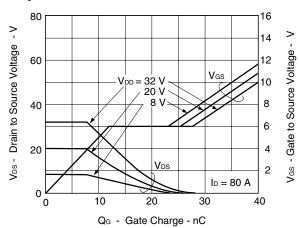


Figure 17. DYNAMIC INPUT/OUTPUT CHARACTERISTICS

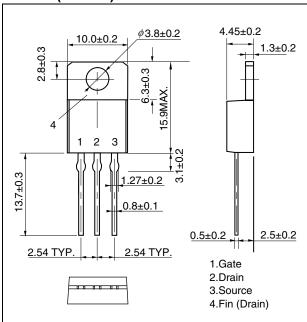


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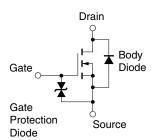


PACKAGE DRAWINGS (Unit: mm)

TO-220 (MP-25K)



EQUIVALENT CIRCUIT



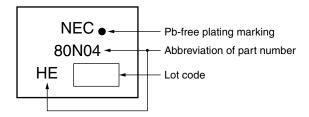
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

6



MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

Process	Conditions	Symbol
Wave soldering	Maximum temperature (Solder temperature): 260°C or below	THDWS
	Time: 10 s or less	
	Maximum chlorine content of rosin flux: 0.2% (wt.) or less	
Partial heating	Maximum temperature (Pin temperature): 350°C or below	
	Time (per one pin): 3 s or less	_
	Maximum chlorine content of rosin flux: 0.2% (wt.) or less	

Data Sheet D17860EJ2V0DS 7

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