August 10, 2009

CP2120 Revision 1.0 Errata

Errata Status Summary

Errata #	Title	Impact	Status	
			Affected Revisions	Fixed Revision
1	Inter-byte delay requirements for read commands on SPI bus.	Minor	Revision 1.0	Not Fixed
2	I^2C write delays with I^2C timeout and bus-free detect disabled.	Minor	Revision 1.0	Not Fixed

Impact Definition: Each erratum is marked with an impact, as defined below:

- Minor—Workaround exists.
- Major—Errata that do not conform to the data sheet or standard.
- Information—The device behavior is not ideal but acceptable. Typically, the data sheet will be changed to match the device behavior.

Errata Details

1. **Description** : Within certain timing constraints, a read command performed via the SPI interface may fail and return invalid information. Intermittent failure to read the requested information can occur if the inter-byte delay before and after the dummy byte in the SPI register read command falls between 0.55 µs and 2.0 µs. The delay between SPI bytes is defined as the time between the last rising edge of SCLK on one byte and the first falling edge of SCLK on the next byte.

   Impact : At certain SPI clock frequencies, or in systems which insert a specific delay between bytes, SPI reads may fail.

   Workaround : Ensure that the inter-byte delay before and after the dummy byte in read transfers are both shorter than 0.55 µs or longer than 2.0 µs.

2. **Description** : When both the I2CTO Timer and I^2C bus-free timeouts are disabled, all I^2C write transactions will take at least 200 ms to execute.

   Impact : This will add significant delays whenever I^2C writes are used.

   Workaround : Enable bus-free timeouts, or enable the I2CTO Timer.