October 21, 2004

CP2102 Rev. B Errata

Silicon Laboratories is pleased to provide samples of the CP2102 revision B. These samples correspond to the CP2102 data sheet revision 1.0. The following errata in performance have been identified with revision B:

Before installation on the PCB the D+/D- USB Pin ESD performance fails above ±1700 V HBM. After PCB assembly, the ESD performance is acceptable assuming one or more standard 0.1 µF power supply decoupling caps are present.

Recommend:
15 kV Schottky Protection Devices to USB I/O as part of customer board design

All errata listed above correspond to revision 1.0 data sheet and will fully comply with the data sheet specifications in the revision C silicon.