

STEVAL-MKI109V1

STM32-based MEMS motherboard compatible with all ST MEMS adapters

Data brief

Features

- Compatible with all available ST MEMS adapter boards
- Controlled by the STM32F102R8 highperformance ARM CortexTM-M3 microcontroller
- Includes a DIL24 socket for easy MEMS adapter connection
- 3 V on-board linear voltage regulator
- DFU compatible for USB microprocessor firmware update
- USB 2.0 full-speed compliant
- Debugging connector for SWD/JTAG

RoHS compliant **Description**

The STEVAL-MKI109V1 is a motherboard designed to provide users with a complete, readyto-use platform for the evaluation of STMicroelectronics' MEMS products.

The board features a DIL24 socket to mount all available adapters for both digital and analog output MEMS devices.

The motherboard includes a high-performance 32-bit microcontroller, which functions as a bridge between the sensor and a PC, on which it is possible to use the downloadable graphical user interface (GUI), or dedicated software routines for customized applications.

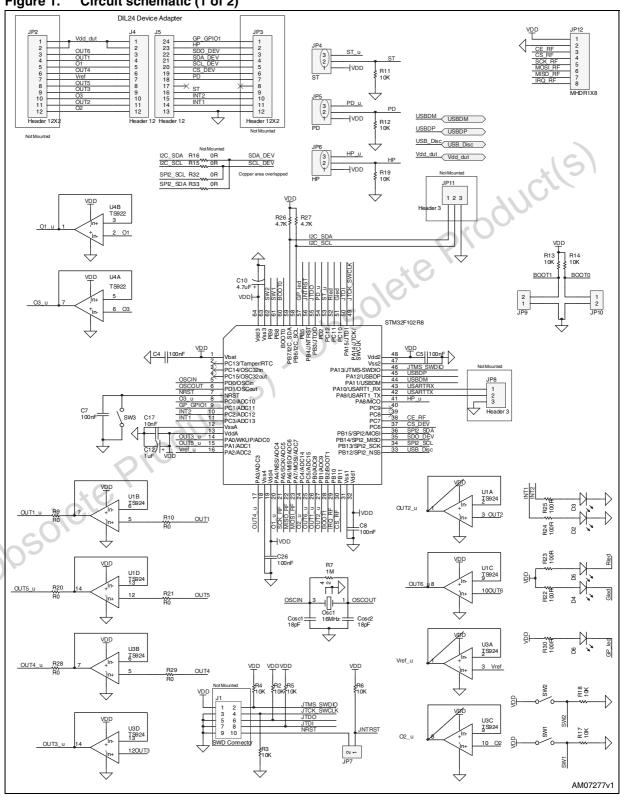


STEVAL-MKI109V1

Schematic diagrams STEVAL-MKI109V1

Schematic diagrams 1

Figure 1. Circuit schematic (1 of 2)



USB_5V 1 TP1 Power Supply VDD Vdd<u>d</u>ut 2 lds3985xx30 U2 Vin BYPASS ΕN C13 10uF __C3 __ 100nF / 100nF _ C14 (TANT.) 33nF | | | R8 | 10k Q1 BC817 Notmounted | | | | | | | | | ₹ R34 36k BC817 √ GND R35 180R R36 1.5k √ GND GND

C6 | 100nF Josole te P R37_____22R USBDM VO1 GND Vbus USBDP VO2 VO2 R38 22R USBLC6-2P6 USB_5V DP nc 10uF -GND Mini-USB B ∯ GND USBDM USBDM USBDP USB_Disc USB_Disc Vdd_dut Vdd_dut AM07278v1

Figure 2. Circuit schematic (2 of 2)

Revision history STEVAL-MKI109V1

2 Revision history

Table 1. Document revision history

Date	Date Revision	on Changes
16-Jun-2010	16-Jun-2010 1	Initial release.
18-Aug-2010	18-Aug-2010 2	-Enlarged and reoriented schematic diagrams in <i>Figure 1</i> and <i>Figure 2</i> to improve readabilityMinor text correction in <i>Figure 1</i> .
Minor text correction in Figure 1. Minor text correction in Figure 1. Minor text correction in Figure 1.		

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