



# BT258S-800R

Logic level thyristor

22 July 2013

Product data sheet

## 1. General description

Planar passivated Silicon Controlled Rectifier (SCR) in a SOT428 (DPAK) surface mountable plastic package intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

## 2. Features and benefits

- Direct interfacing with low power drivers and microcontrollers
- High bidirectional blocking voltage capability
- High thermal cycling performance
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate suitable for logic level controls
- Surface mountable package

## 3. Applications

- General purpose switching and phase control
- Protection circuits
- Ignition circuits, CDI for 2- and 3-wheelers
- Motor control - e.g. small kitchen appliances

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	-	800	V
$V_{RRM}$	repetitive peak reverse voltage		-	-	800	V
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 10\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	-	75	A
$T_j$	junction temperature	[1]	-	-	125	$^{\circ}\text{C}$
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 111\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a>	-	-	8	A

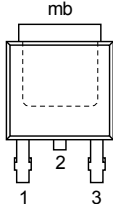



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>	-	50	200	$\mu\text{A}$
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; $R_{GK} = 100\text{ }\Omega$ ; exponential waveform; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); <a href="#">Fig. 13</a>	50	100	-	$\text{V}/\mu\text{s}$

[1] Operation above junction temperatures of  $110\text{ }^\circ\text{C}$  may require the use of a gate to cathode resistor of  $1\text{ k}\Omega$

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 <p><b>DPAK (SOT428)</b></p>	
2	A	anode		
3	G	gate		
mb	A	mounting base; connected to anode		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT258S-800R	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

## 7. Limiting values

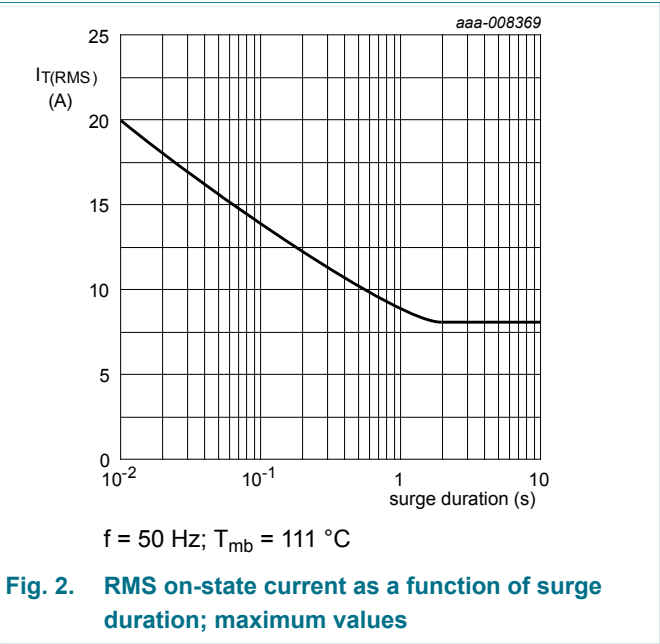
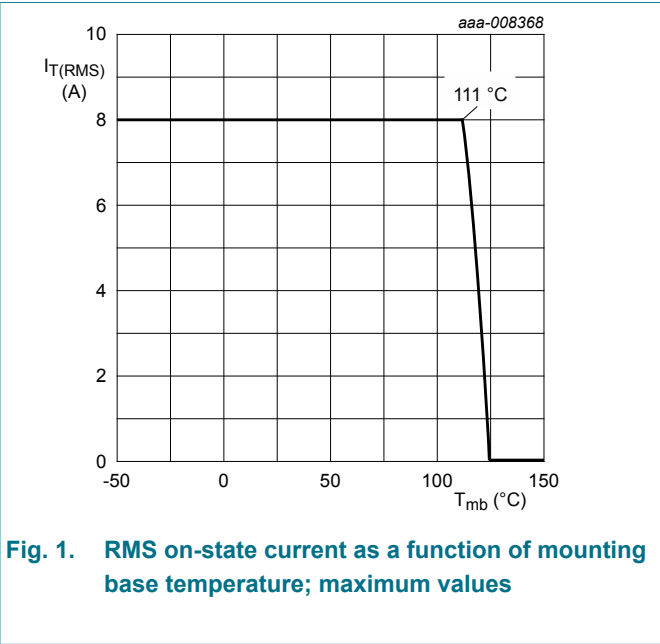
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	800	V
$V_{RRM}$	repetitive peak reverse voltage		-	800	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 111\text{ }^\circ\text{C}$ ; <a href="#">Fig. 3</a>	-	5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 111\text{ }^\circ\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a>	-	8	A
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; $t_p = 10\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	75	A

Symbol	Parameter	Conditions		Min	Max	Unit
		half sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 8.3\text{ ms}$		-	82	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$ ; sine-wave pulse		-	28	$\text{A}^2\text{s}$
$dl_T/dt$	rate of rise of on-state current	$I_T = 10\text{ A}$ ; $I_G = 50\text{ mA}$ ; $dl_G/dt = 50\text{ mA}/\mu\text{s}$		-	50	$\text{A}/\mu\text{s}$
$I_{GM}$	peak gate current			-	2	A
$V_{RGM}$	peak reverse gate voltage			-	5	V
$P_{GM}$	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
$T_{stg}$	storage temperature			-40	150	$^{\circ}\text{C}$
$T_j$	junction temperature		[1]	-	125	$^{\circ}\text{C}$

[1] Operation above junction temperatures of 110 °C may require the use of a gate to cathode resistor of 1 kΩ



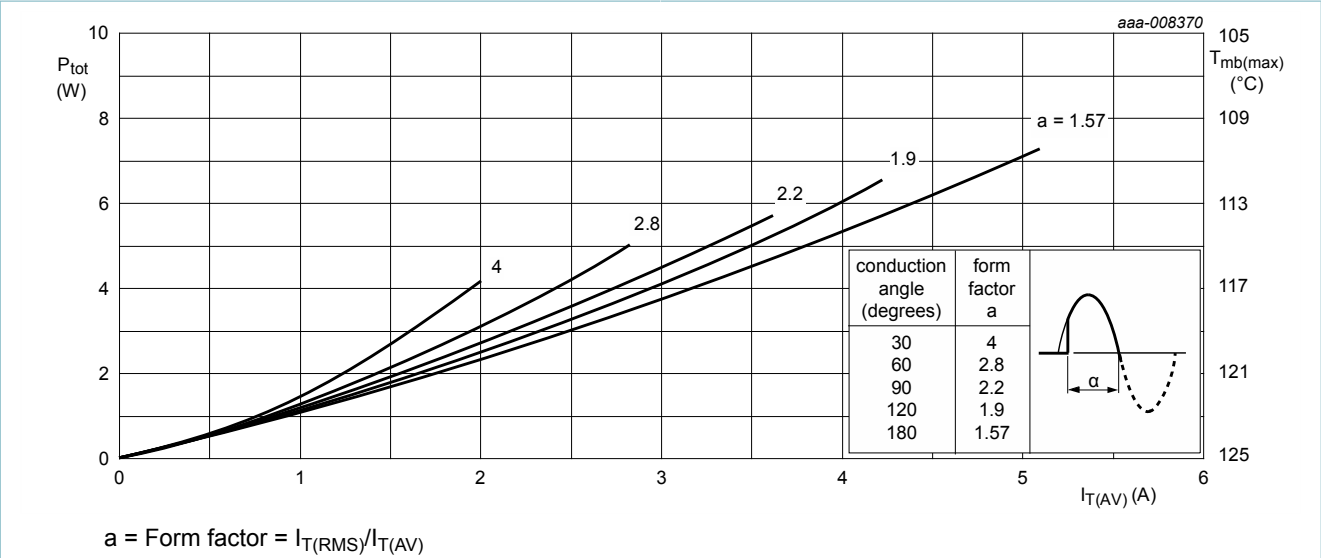


Fig. 3. Total power dissipation as a function of average on-state current; maximum values

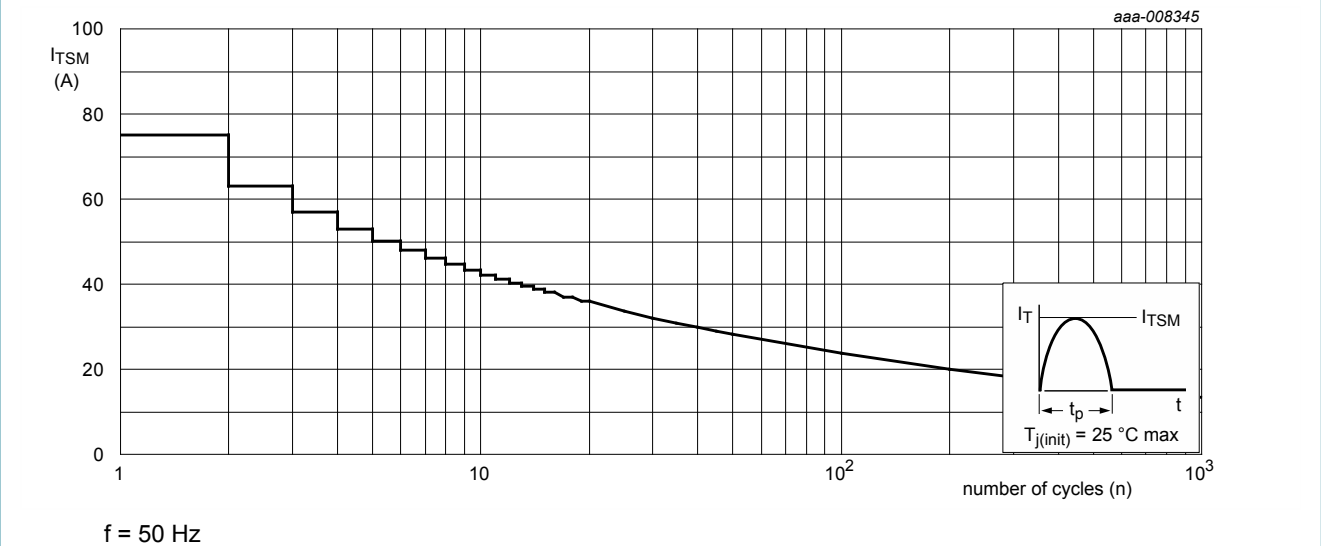
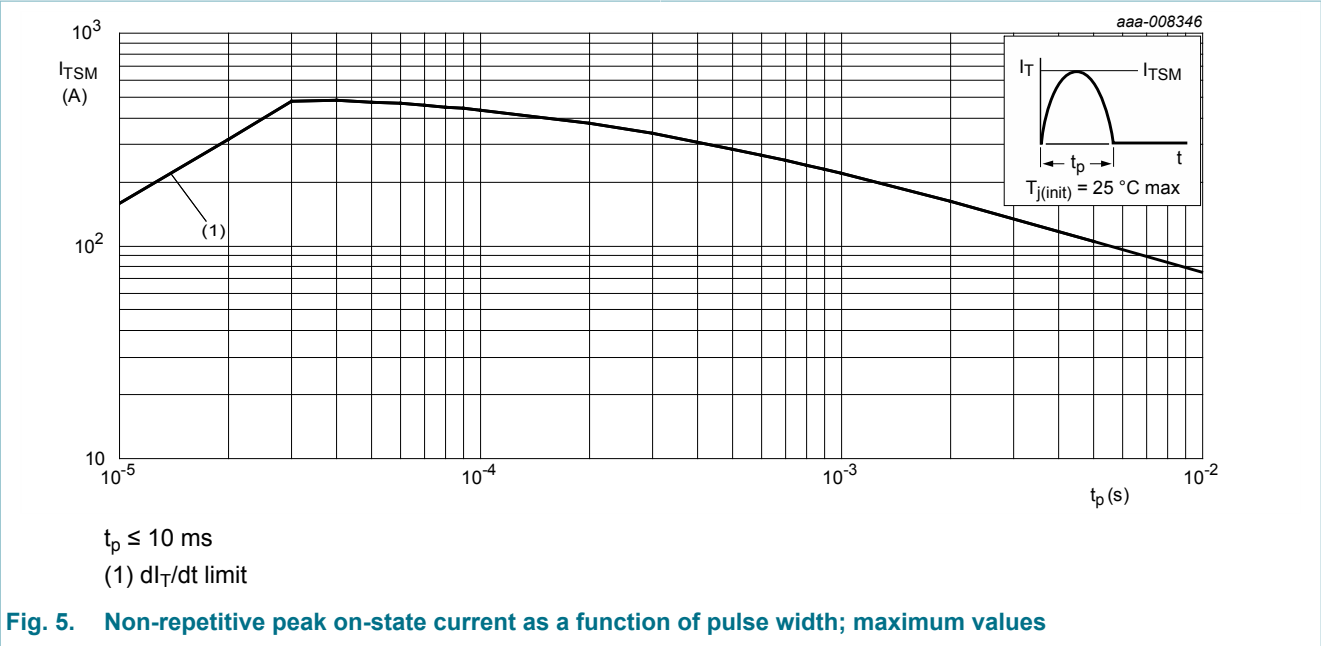


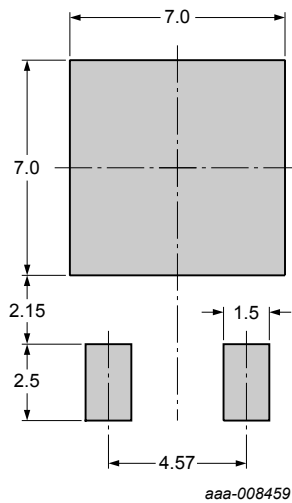
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 7</a>	-	-	2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Device mounted on an FR4 printed-circuit board, single-sided copper, tin-plated and standard footprint; <a href="#">Fig. 6</a>	-	75	-	K/W



All dimensions are in mm  
Plastic meets requirements of UL94 V-O at 3.175 mm

Fig. 6. SOT428: minimum pad sizes for surface-mounting

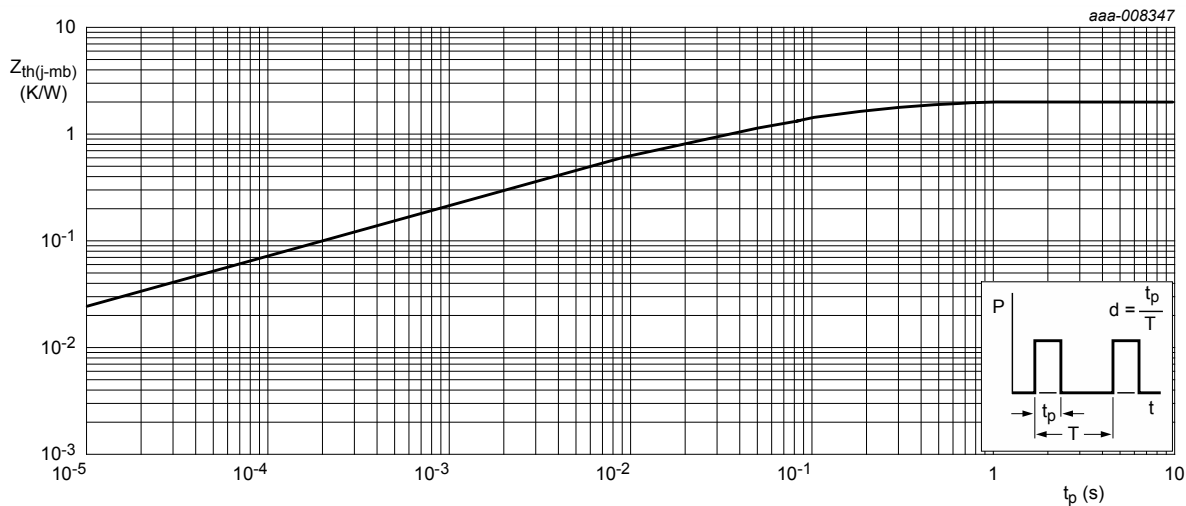


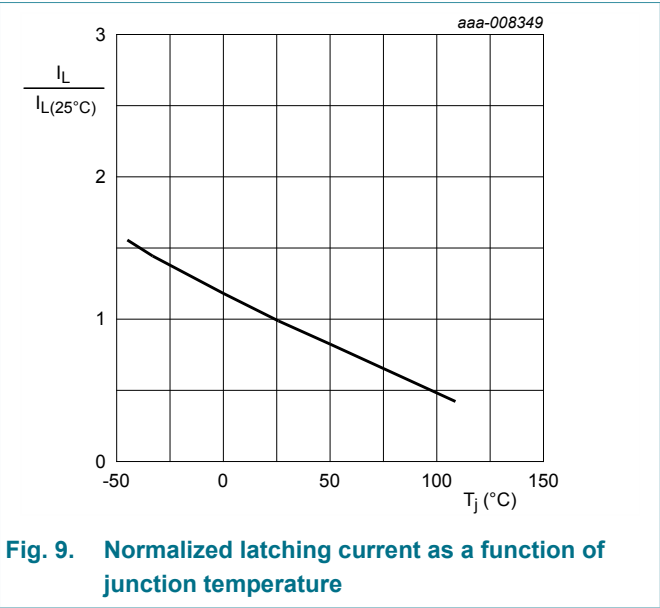
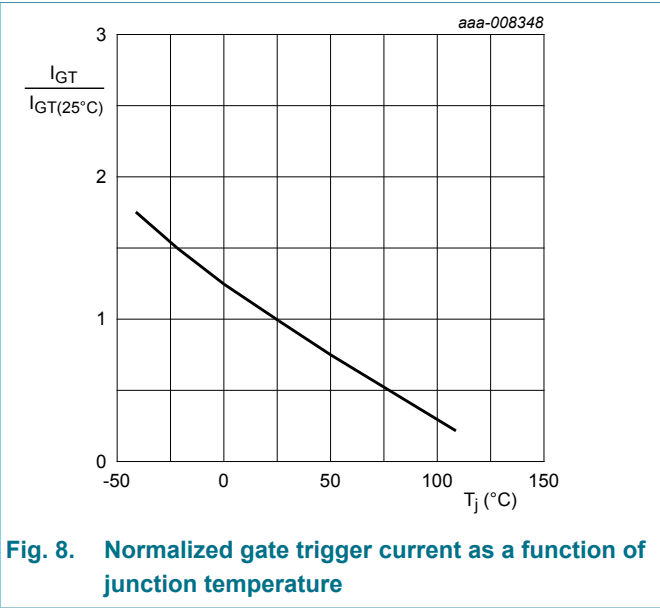
Fig. 7. Transient thermal impedance from junction to mounting base as a function of pulse width

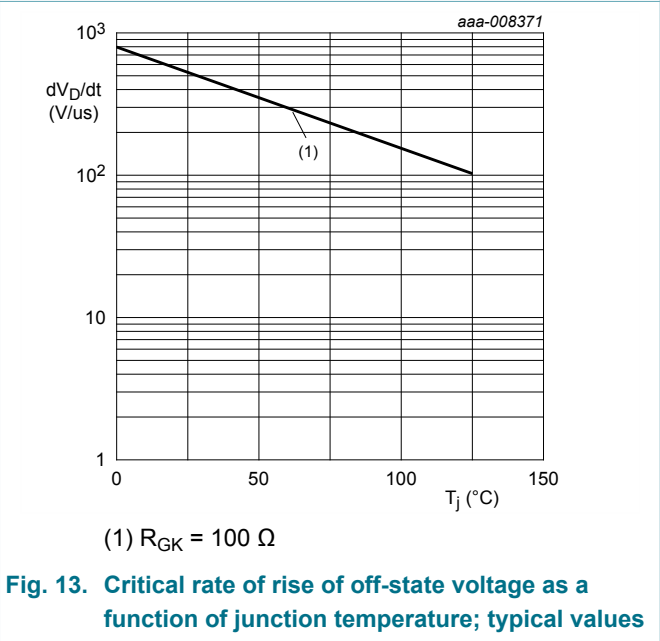
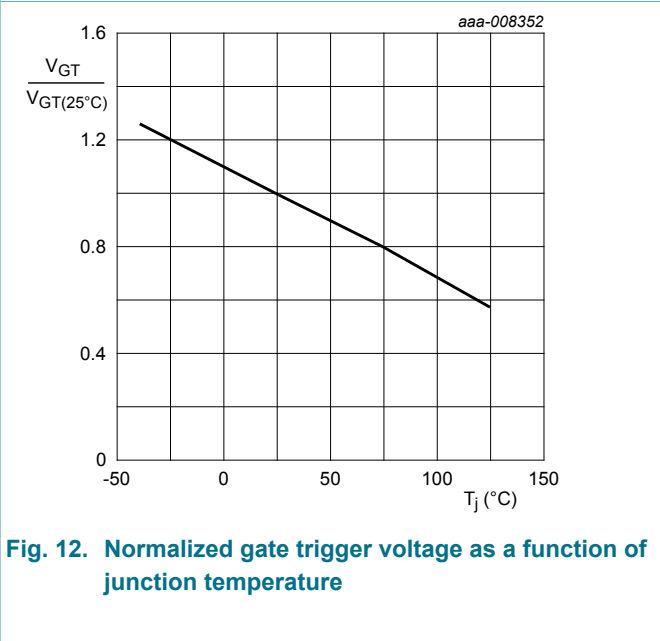
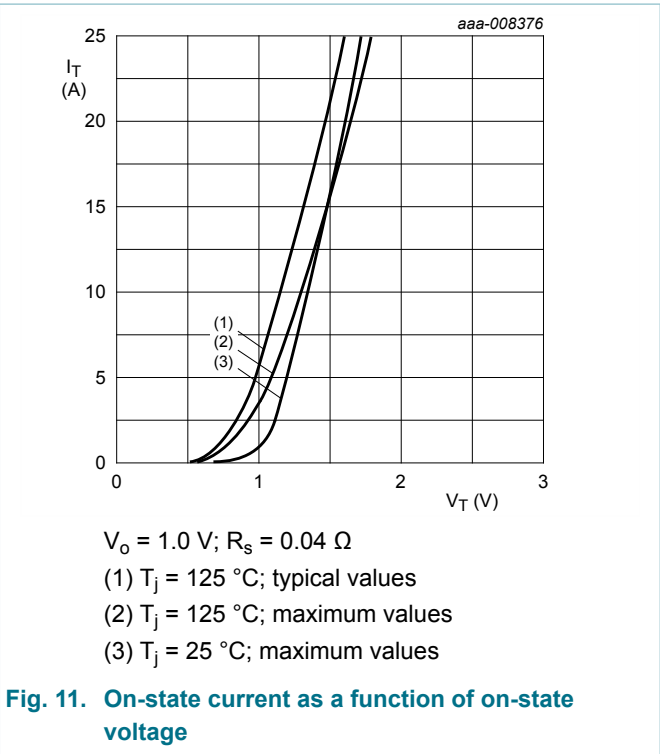
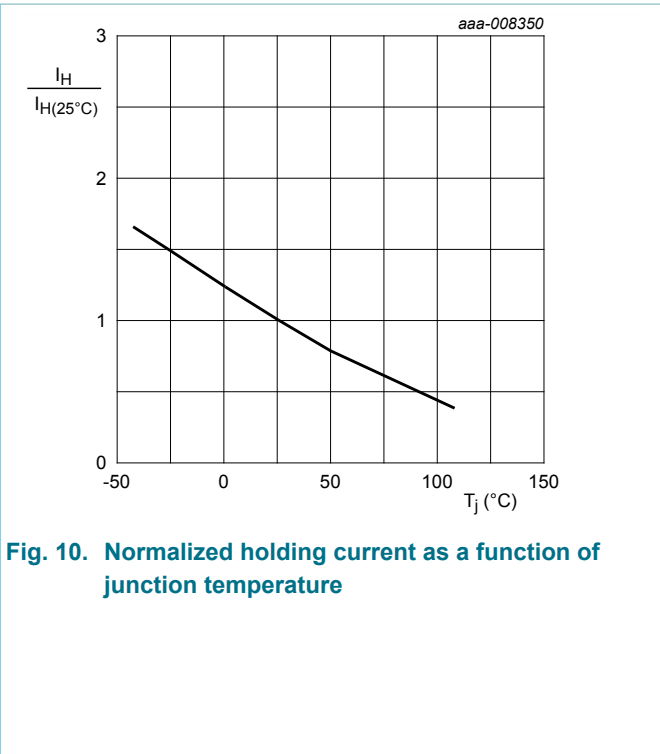
9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ }^{\circ}\text{C}$ ; Fig. 8	-	50	200	$\mu\text{A}$
$I_L$	latching current	$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; $T_j = 25\text{ }^{\circ}\text{C}$ ; Fig. 9	-	0.4	10	$\text{mA}$
$I_H$	holding current	$V_D = 12\text{ V}$ ; $T_j = 25\text{ }^{\circ}\text{C}$ ; Fig. 10	-	0.3	6	$\text{mA}$
$V_T$	on-state voltage	$I_T = 16\text{ A}$ ; $T_j = 25\text{ }^{\circ}\text{C}$ ; Fig. 11	-	1.3	1.6	$\text{V}$
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ }^{\circ}\text{C}$ ; Fig. 12	-	0.4	1	$\text{V}$

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		$V_D = 800\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 110\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 12</a>		0.1	0.2	-	V
$I_D$	off-state current	$V_D = 800\text{ V}$ ; $T_j = 125\text{ }^{\circ}\text{C}$		-	0.1	0.5	mA
$I_R$	reverse current	$V_R = 800\text{ V}$ ; $T_j = 125\text{ }^{\circ}\text{C}$		-	0.1	0.5	mA
Dynamic characteristics							
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$ ; $T_j = 125\text{ }^{\circ}\text{C}$ ; $R_{GK} = 100\text{ }\Omega$ ; exponential waveform; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); <a href="#">Fig. 13</a>		50	100	-	V/ $\mu$ s
$t_{gt}$	gate-controlled turn-on time	$I_{TM} = 10\text{ A}$ ; $V_D = 800\text{ V}$ ; $I_G = 5\text{ mA}$ ; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$ ; $T_j = 25\text{ }^{\circ}\text{C}$		-	2	-	$\mu$ s
$t_q$	commutated turn-off time	$V_{DM} = 536\text{ V}$ ; $T_j = 125\text{ }^{\circ}\text{C}$ ; $I_{TM} = 12\text{ A}$ ; $V_R = 24\text{ V}$ ; $(dI_T/dt)_M = 10\text{ A}/\mu\text{s}$ ; $dV_D/dt = 2\text{ V}/\mu\text{s}$ ; $R_{GK} = 1\text{ k}\Omega$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ )		-	100	-	$\mu$ s







10. Package outline

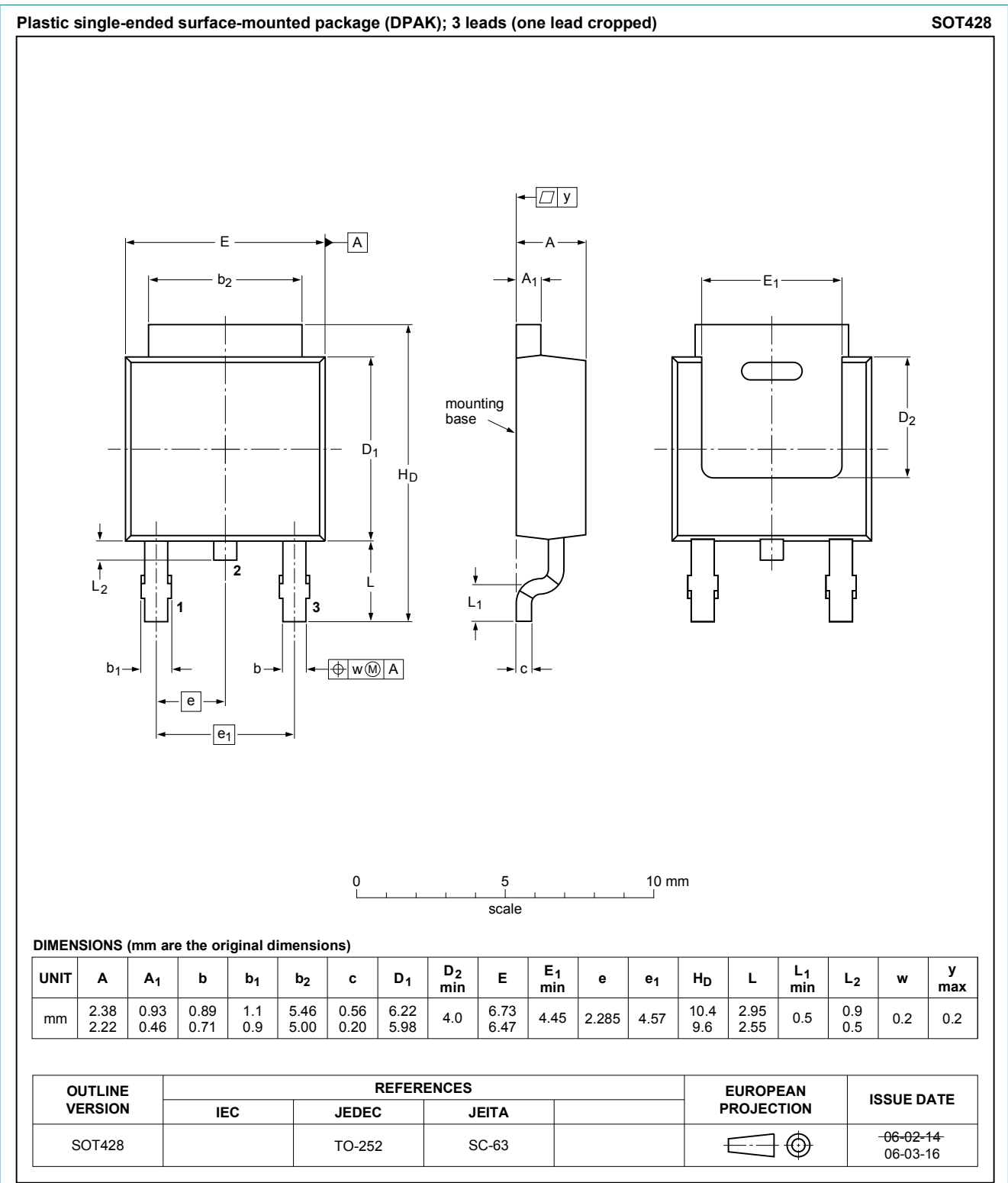
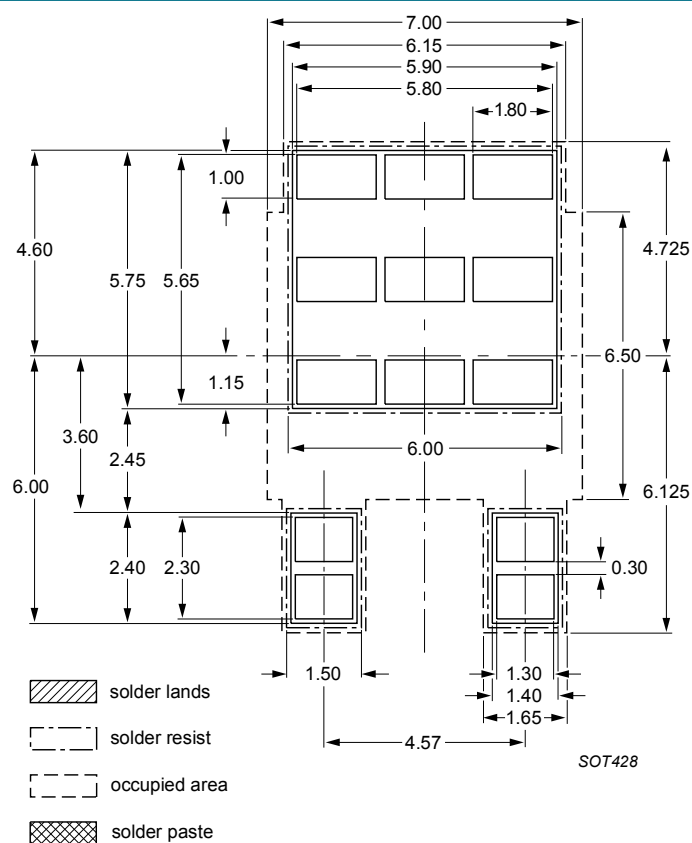


Fig. 14. Package outline DPAK (SOT428)

## 11. Soldering



**Fig. 15. Reflow soldering footprint for DPAK (SOT428)**

## 12. Legal information

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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