



# SEARAY CONNECTOR ROUTING GUIDE

## SEARAY™\* Board To Board System Connector Routing Guide



\* SEARAY is a trademark of Samtec Inc

REVISION: <b>A</b>	ECR/ECN INFORMATION: EC No: <b>UCP2010-1365</b> DATE: <b>2009/12/01</b>	TITLE: <b>SEARAY BOARD TO BOARD SYSTEM CONNECTOR ROUTING GUIDE</b>	SHEET No. <b>1 of 14</b>
DOCUMENT NUMBER: <b>AS-45970-990</b>	CREATED / REVISED BY: <b>GREGORI</b>	CHECKED BY: <b>SQUIRE / STANCZAK</b>	APPROVED BY: <b>COMERCI</b>

FILENAME: PS74031C.DOC



# SEARAY CONNECTOR ROUTING GUIDE

## TABLE OF CONTENTS

<b>I. <u>Overview of the Connector</u></b>	<b>3</b>
<b>II. <u>Routing Recommendations</u></b>	<b>4</b>
<b>PCB Pad Layout / Connector foot print</b>	<b>4</b>
Figure 1: Plug Connector Solder Pad Layout	4
Figure 2: Receptacle Connector Solder Pad Layout	4
<b>Routing Pattern: Trace Geometry</b>	<b>5</b>
Figure 3: 5-5-5 Trace Geometry	5
Figure 4: Lateral Escape Routing	6
Figure 5: Longitudinal Escape Routing	6
<b>Pair to Pair Spacing When Out of Pin Field</b>	<b>7</b>
Figure 6: Trace Expansion Out of Pin Field	7
<b>Grounding Patterns</b>	<b>7</b>
Figure 7: Grounding Patterns	8
Figure 8: Shielded Grounding Patterns	8
<b>Pad and Anti-Pad Guidelines</b>	<b>9</b>
Figure 9: Trace Routing	9
<b>Via Construction</b>	<b>10</b>
Figure 10: Via Construction Used in SI Analysis	10
<b>Differential Trace to Signal Pad Attachment</b>	<b>10</b>
Figure 11: Flag Escape Detail Longitudinal Escape	10
<b>Intra-pair and Inter-pair skew control</b>	<b>11</b>
Figure 12: Flag Escape Detail	11
<b>Depth of Rows</b>	<b>11</b>
<b>Layer Allocation</b>	<b>12</b>
<b>III. <u>Crosstalk Tx and Rx Arrangement</u></b>	<b>12</b>
Table A: TX RX grouping separated by low speed (LS) signal columns	12
Table B: TX RX pairs separated by low speed (LS) signal columns	13
<b>Back Drilling</b>	<b>13</b>
Figure 13: Back Drill Specification	13
<b>Keep Out Area</b>	<b>14</b>

REVISION:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
<b>A</b>	EC No: UCP2010-1365	<b>SEARAY BOARD TO BOARD SYSTEM CONNECTOR ROUTING GUIDE</b>	<b>2 of 14</b>
DATE: 2009/12/01			
DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
<b>AS-45970-990</b>	<b>GREGORI</b>	<b>SQUIRE / STANCZAK</b>	<b>COMERCI</b>



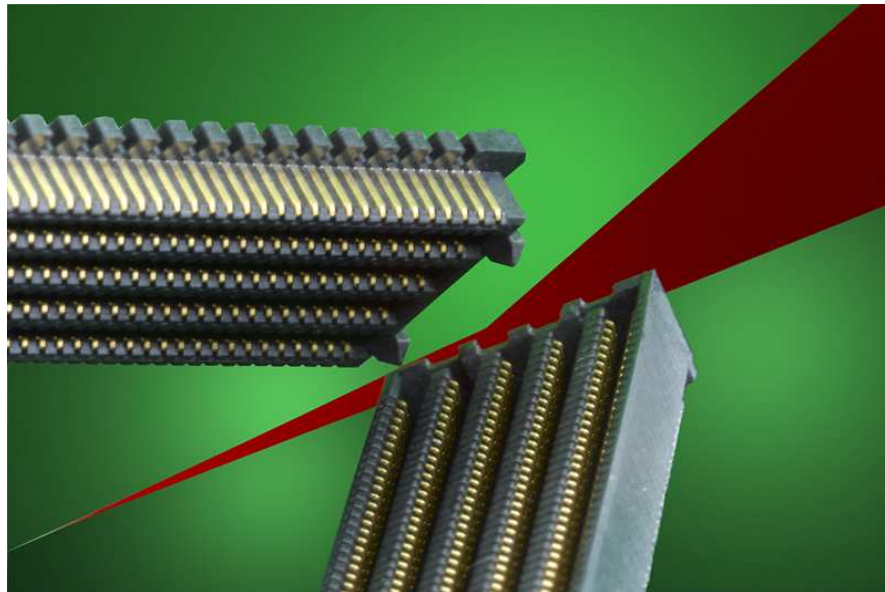
# SEARAY CONNECTOR ROUTING GUIDE

## I. OVERVIEW OF THE CONNECTOR

The SEARAY connector system provides data rates up to 15 Gbps and superior signal density up to 67 differential pairs per inch. The SEARAY open pin field provides designers with flexibility in signal allocation for high-speed differential pairs, low speed single ended lines and power.

SEARAY's recessed housing protects terminals from stubbing during mating and the shrouded housing with guide pins helps align mezzanine cards in blind mating situations. In processing, SEARAY benefits from Solder Charge<sup>TM</sup> SMT Technology with many advantages over BGA such as increased PCB retention, easier x-ray inspection and more reliable interfacing to the PCB with a riveted terminal ensuring contact with the solder pad.

The SEARAY connector system is designed for mezzanine architectures to meet the growing demands of next-generation telecommunication and data networking equipment manufacturers. The SEARAY connector system is offered in a large variety of options with circuit sizes ranging from 40 to 500 circuits and stack heights covering the gamete of 7 to 15mm.



REVISION:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
<b>A</b>	EC No: <b>UCP2010-1365</b> DATE: <b>2009/12/01</b>	<b>SEARAY BOARD TO BOARD SYSTEM CONNECTOR ROUTING GUIDE</b>	<b>3 of 14</b>
DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
<b>AS-45970-990</b>	<b>GREGORI</b>	<b>SQUIRE / STANCZAK</b>	<b>COMERCI</b>



# SEARAY CONNECTOR ROUTING GUIDE

## II. ROUTING RECOMMENDATIONS

### PCB Pad Layout / Connector Footprint

The SEARAY connector system is designed for .025" (0.635mm) diameter solder pads. A simple .050" x .050" (1.27mm x 1.27mm) solder pad grid is shown in Figure 1. The solder pad layout is identical between the plug and receptacle with the exception of the non-plated thru holes (NPTH) for connector alignment pegs relative to row 1 / position 1.

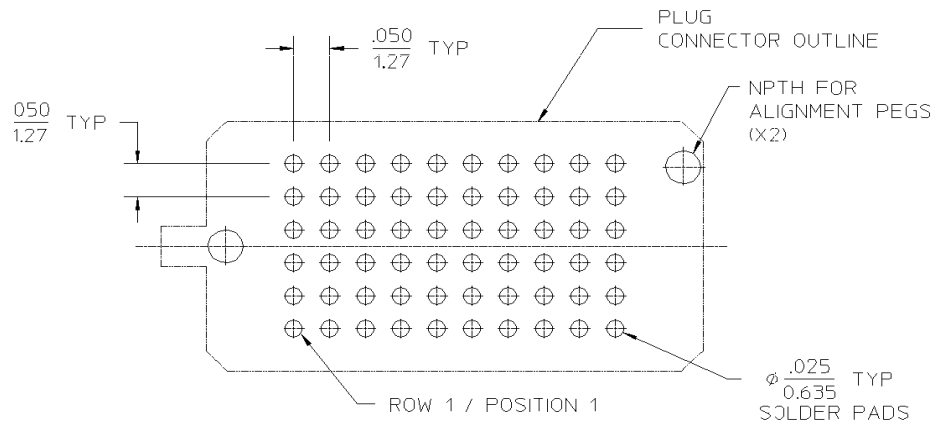


Figure 1: Plug Connector Solder Pad Layout

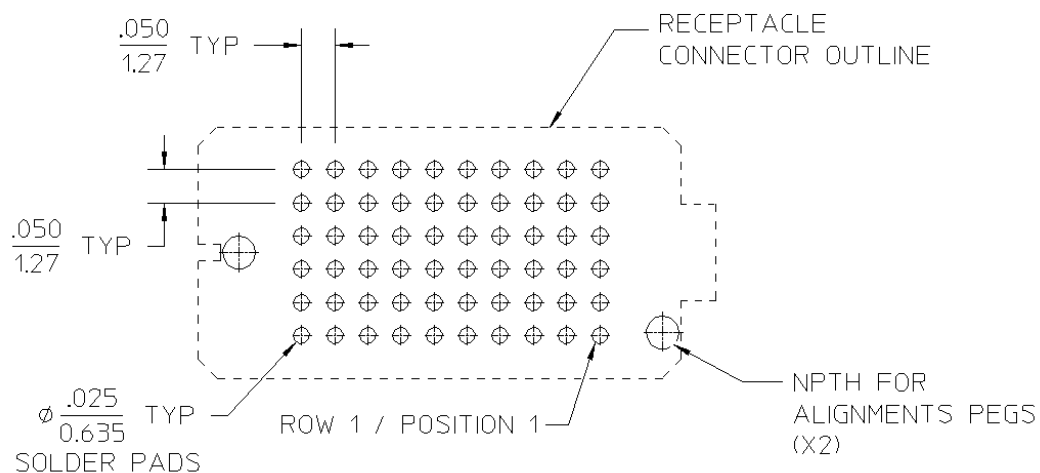


Figure 2: Receptacle Connector Solder Pad Layout

REVISION:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
<b>A</b>	EC No: <b>UCP2010-1365</b> DATE: <b>2009/12/01</b>	<b>SEARAY BOARD TO BOARD SYSTEM CONNECTOR ROUTING GUIDE</b>	<b>4 of 14</b>
DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
<b>AS-45970-990</b>	<b>GREGORI</b>	<b>SQUIRE / STANCZAK</b>	<b>COMERCI</b>



# SEARAY CONNECTOR ROUTING GUIDE

## Routing Pattern: Trace Geometry

For high speed applications it is recommended that the differential signals be routed through the via pin field as tightly coupled differential pairs in order to minimize the effects of crosstalk. The differential impedance of the pair should be tuned to be as close to the nominal system impedance as possible (typically 100 ohms). Other parameters such as common mode impedance, fabrication consistency, attenuation, and routing density may also influence the choice of trace dimensions for a particular application.

For the SEARAY connector the allowable trace geometry is bounded by the minimum dimensions constant with required impedance and fabrication capabilities and by the maximum allowable by the SEARAY pin field grid dimensions .050" x .050" (1.27mm x 1.27mm) of the solder pad grid. A 5-5-5 mil trace geometry is recommended within the via pin field. Other traces geometries may be used, but it is recommended that the total differential pair width be restricted to 15mils or less. Outside the via pin field the traces may be expanded as a loosely coupled differential pair (for example 7-14-7) or uncoupled single ended traces as required by the application. It is recommended that the pairs be edge coupled and aligned parallel to the long axis of the connector. While broad side coupling may be used, it is likely to require additional skew compensation.

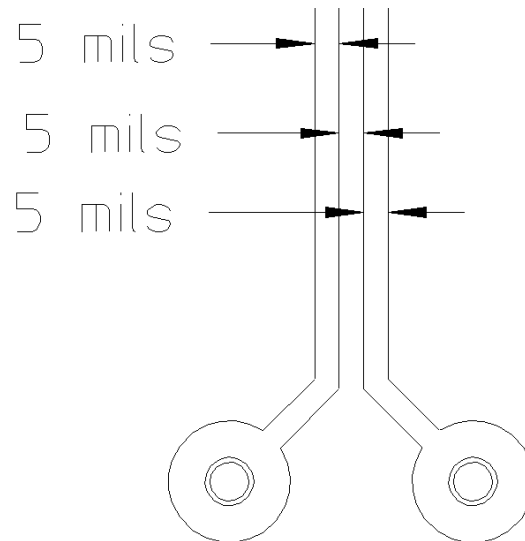


Figure 3: 5-5-5 Trace Geometry

<u>REVISION:</u>  <b>A</b>	<u>ECR/ECN INFORMATION:</u> <u>EC No:</u> <b>UCP2010-1365</b> <u>DATE:</u> <b>2009/12/01</b>	<u>TITLE:</u>  <b>SEARAY BOARD TO BOARD SYSTEM CONNECTOR ROUTING GUIDE</b>			<u>SHEET No.</u>  <b>5 of 14</b>
<u>DOCUMENT NUMBER:</u>  <b>AS-45970-990</b>		<u>CREATED / REVISED BY:</u>  <b>GREGORI</b>	<u>CHECKED BY:</u>  <b>SQUIRE / STANCZAK</b>	<u>APPROVED BY:</u>  <b>COMERCI</b>	
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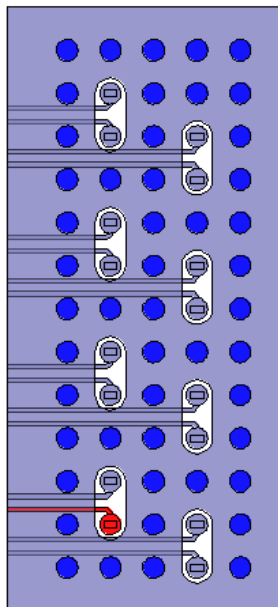


Figure 4: Lateral Escape Routing

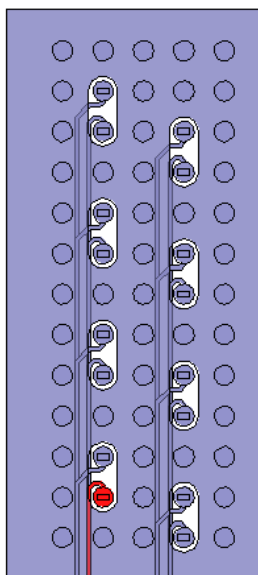


Figure 5: Longitudinal Escape Routing

REVISION:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
<b>A</b>	EC No: <b>UCP2010-1365</b> DATE: <b>2009/12/01</b>	<b>SEARAY BOARD TO BOARD SYSTEM CONNECTOR ROUTING GUIDE</b>	<b>6 of 14</b>
DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
<b>AS-45970-990</b>	<b>GREGORI</b>	<b>SQUIRE / STANCZAK</b>	<b>COMERCI</b>



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## Pair To Pair Spacing When Out of Pin Field

Outside of the pin field it is recommended that the pair to pair spacing be as wide as possible to minimize the pair to pair cross talk. Transitions from the pin field tracing spacing to the general board trace structure should be performed smoothly and symmetrically.

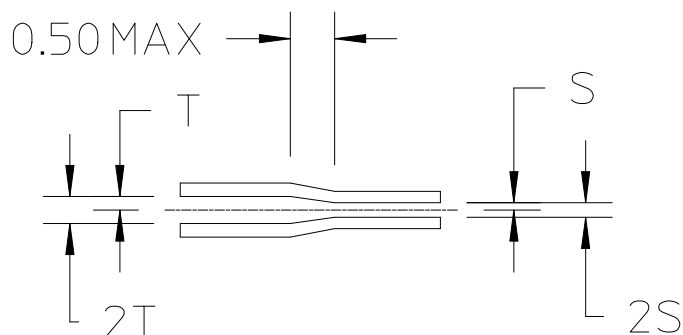


Figure 6: Trace Expansion Out of Pin Field

## Grounding Patterns

The SEARAY connector being an open pin field connector allows various arrangements of signal pins and ground pins to be defined. For maximum density a staggered 2:1 signal / ground arrangement may be used. It should be noted that this arrangement may lead to higher crosstalk than other arrangements.

A staggered 1:1 signal / ground arrangement may be used to give improved crosstalk isolation relative to the 2:1 signal / ground arrangement.

For maximum crosstalk isolation a fully shielded ground pattern can be used at the expense of signal density.

REVISION: <b>A</b>	ECR/ECN INFORMATION: EC No: <b>UCP2010-1365</b> DATE: <b>2009/12/01</b>	TITLE: <b>SEARAY BOARD TO BOARD SYSTEM CONNECTOR ROUTING GUIDE</b>	SHEET No. <b>7 of 14</b>
DOCUMENT NUMBER: <b>AS-45970-990</b>	CREATED / REVISED BY: <b>GREGORI</b>	CHECKED BY: <b>SQUIRE / STANCZAK</b>	APPROVED BY: <b>COMERCI</b>



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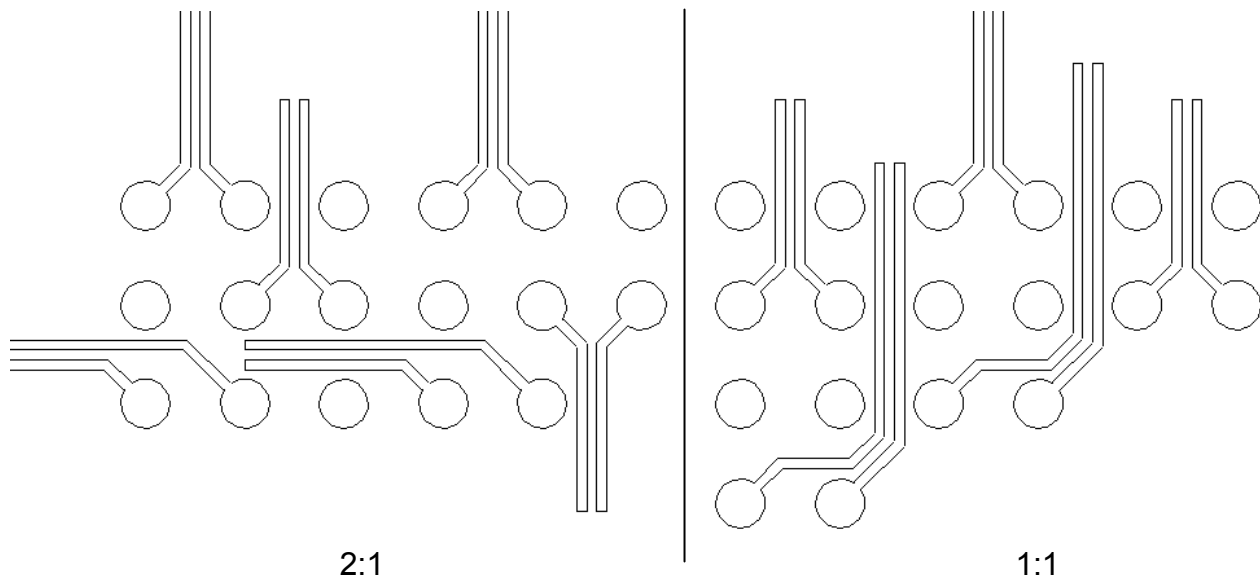


Figure 7: Grounding Patterns

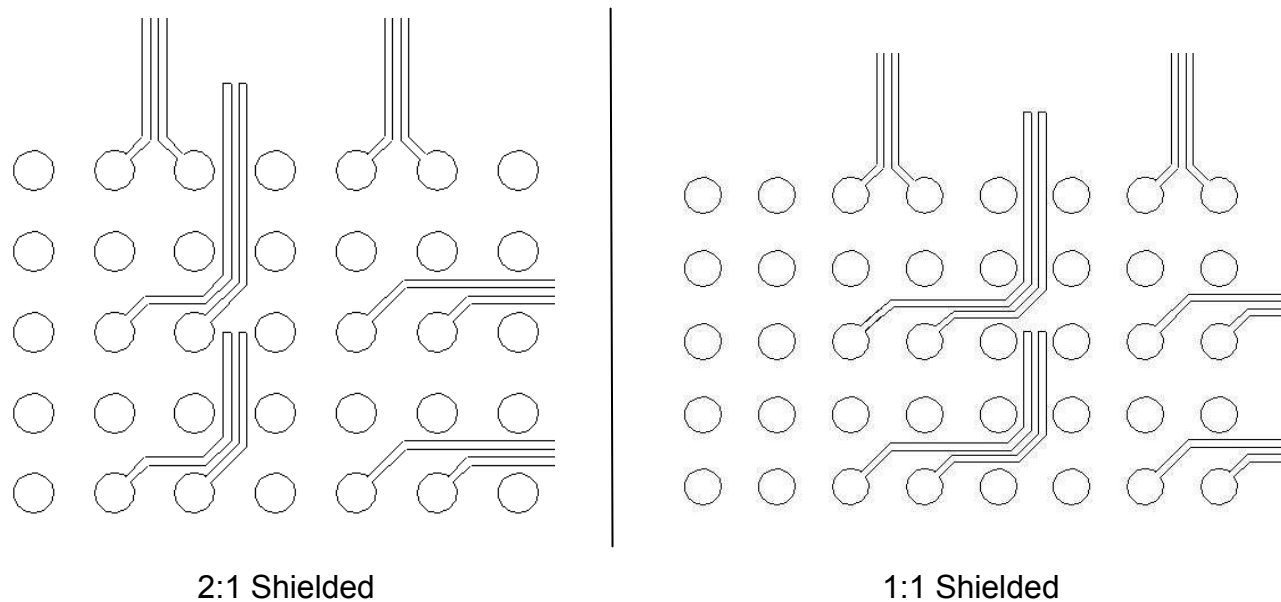


Figure 8: Shielded Grounding Patterns

REVISION:	ECR/ECN INFORMATION:	TITLE:			SHEET No.
A	EC No: UCP2010-1365 DATE: 2009/12/01	SEARAY BOARD TO BOARD SYSTEM CONNECTOR ROUTING GUIDE			8 of 14
DOCUMENT NUMBER: AS-45970-990		CREATED / REVISED BY: GREGORI	CHECKED BY: SQUIRE / STANCZAK	APPROVED BY: COMERCI	





# SEARAY CONNECTOR ROUTING GUIDE

## Pad and Anti-pad guidelines

For High-speed signaling applications Pad and anti-pad construction are of critical importance. For correct attachment of the SEARAY connector the top layer SMT pads are required to be .025" (0.635mm) in diameter. The internal pads should be small to minimize capacitance. The inner layer pads and annular ring with outer diameter of 18 mils is recommended. The number of pads on inner layers should be the minimal required to maintain good adhesion of the via to the PCB in order to minimize the capacitance for the via structure.

Anti-pads are recommended to be 35 mils in radius when used with 15mil (total width) differential pairs (for example 5-5-5 or 4-6-4 traces). The anti-pad should be large to allow for minimum deviation of impedance from the nominal value. However, it should not be so large that the anti-pad cavity can extend over the trace causing impedance discontinuities and a reduction in cross talk isolation. Anti-pads may align with the outer edges of the differential traces, but should not extend over the differential pairs in order maintain control of crosstalk and impedance. Smaller than recommended anti-pads may be used but a negative influence on via impedance is expected.

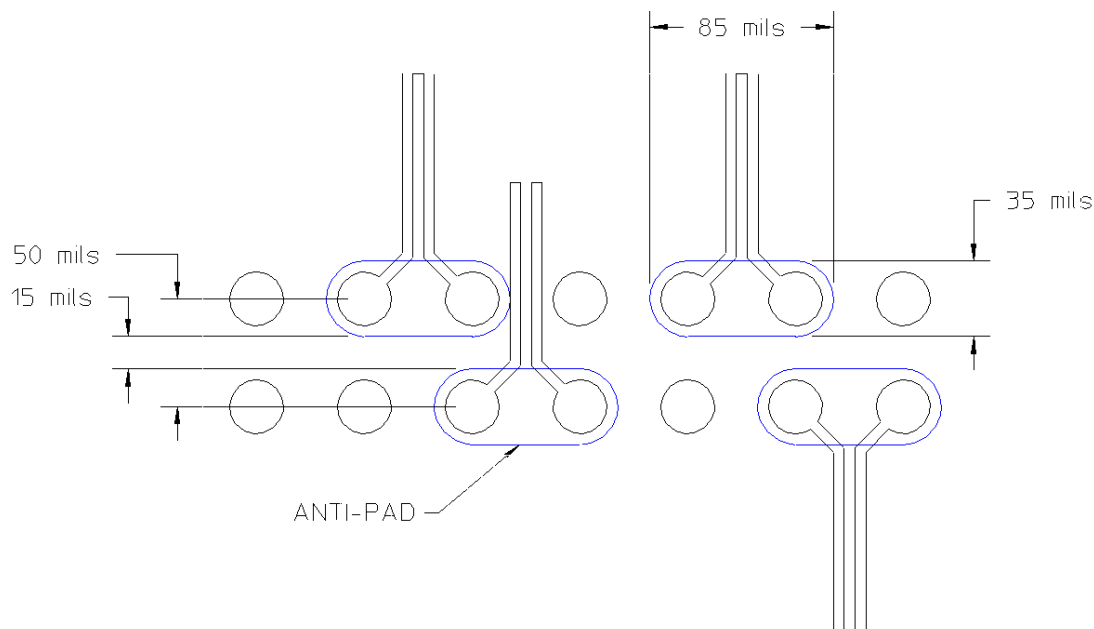


Figure 9: Trace Routing

REVISION:	ECR/ECN INFORMATION:	TITLE:			SHEET No.
<b>A</b>	EC No: <b>UCP2010-1365</b>	<b>SEARAY BOARD TO BOARD SYSTEM CONNECTOR ROUTING GUIDE</b>			<b>9 of 14</b>
DATE: <b>2009/12/01</b>		CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:	
<b>AS-45970-990</b>		<b>GREGORI</b>	<b>SQUIRE / STANCZAK</b>	<b>COMERCI</b>	



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## Via construction

For the SEARAY connector via in pad construction is recommended to minimize any impedance discontinuity at the via / pad transition. Dog bone via structures may be used but with an expected reduction in electrical performance.

As a surface mounted technology (SMT), the SEARAY connector does not constrain the choice of via size due to compliant pin or press fit requirements. A 10 mil (drill) via barrel was used in the SI analysis of the SEARAY via structure and this size or smaller is recommended depending on the host board thickness and allowable aspect ratio.

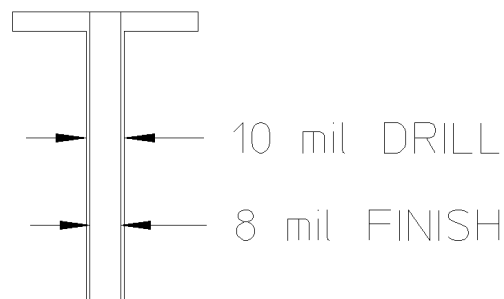


Figure 10: Via Construction Used in SI Analysis

## Differential Trace to Signal Pad Attachment

For the SEARAY connector a 45° flag style launch (Figure 4) is preferred for high speed applications. The 45° flag provides a reduced capacitance and reduced differential impedance discontinuity.

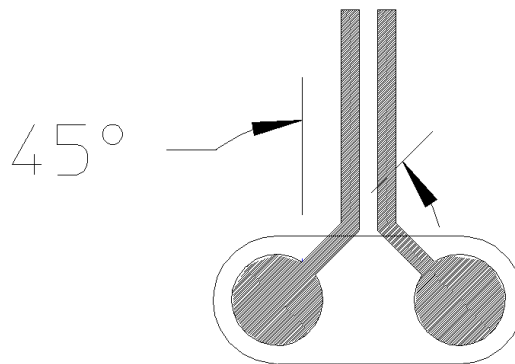


Figure 11: Standard Escape Detail (Longitudinal)

REVISION:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
<b>A</b>	EC No: <b>UCP2010-1365</b> DATE: <b>2009/12/01</b>	<b>SEARAY BOARD TO BOARD SYSTEM CONNECTOR ROUTING GUIDE</b>	<b>10 of 14</b>
DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
<b>AS-45970-990</b>	<b>GREGORI</b>	<b>SQUIRE / STANCZAK</b>	<b>COMERCI</b>



# SEARAY CONNECTOR ROUTING GUIDE

## Intra-pair and Inter-pair skew control

Routing orthogonally to the differential pair directly through the pin field in a lateral escape configuration is recommended to minimize the intra-pair skew. A longitudinal escape may be used but some form of skew compensation may be required. It is recommended that the differential pairs be routed through opposite side of the connector on the top and bottom boards to minimize inter-pair skew. If this is impractical then skew compensation should be performed outside the pin field to achieve an acceptable level of inter-pair skew control. If the traces are routed longitudinally intra-pair skew may be compensated by routing the traces on the top and bottom board in opposite directions so that the traces are essentially mirror image. It is recommended that any skew compensation applied to the traces be distributed along the traces outside of the pin field region rather than performed at a single point along the trace.

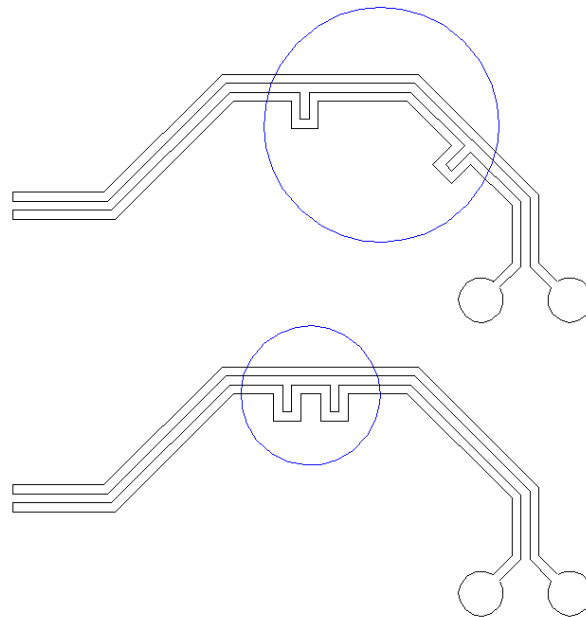


Figure 12: Flag Escape Detail

## Depth of rows

It is recommended that the differential traces be routed to minimize the depth of rows through which the signal traces must pass. This means that ideally the signals be routed with center symmetry along the longitudinal axis of the connector so that cross talk and impedance variations observed by the signal traces are minimized.

REVISION: <b>A</b>	ECR/ECN INFORMATION: EC No: <b>UCP2010-1365</b> DATE: <b>2009/12/01</b>	TITLE: <b>SEARAY BOARD TO BOARD SYSTEM CONNECTOR ROUTING GUIDE</b>	SHEET No. <b>11 of 14</b>
DOCUMENT NUMBER: <b>AS-45970-990</b>	CREATED / REVISED BY: <b>GREGORI</b>	CHECKED BY: <b>SQUIRE / STANCZAK</b>	APPROVED BY: <b>COMERCI</b>



# SEARAY CONNECTOR ROUTING GUIDE

## Layer allocation

To avoid stub effects it is recommended that high speed differential pairs be routed on the bottom layers of the PCB board. Use of embedded micro-strip routing on the top layer and strip-line traces with micro-vias on the upper layers can allow high speed routing on the upper layers with minimum stub effects. Middle layers should be used with caution when routing high speed lines. If middle layer must be used then back drilling is highly recommended to optimize impedance and minimize crosstalk.

## III. CROSSTALK TX AND RX ARRANGEMENT

Cross talk is strongly influenced by the rise time of the input signal. High-speed signals can show significant increase in cross talk relative to lower speed signals in the same channel. For this reason careful consideration of signal arrangement should be made. It is recommended that Tx and Rx signals be grouped together in separate blocks to minimize cross talk. In addition high-speed signals can be separated by power return and low speed signaling to further increase crosstalk isolation. It is also recommended that Tx and Rx signals be routed out on different layers to increase cross talk isolation between traces

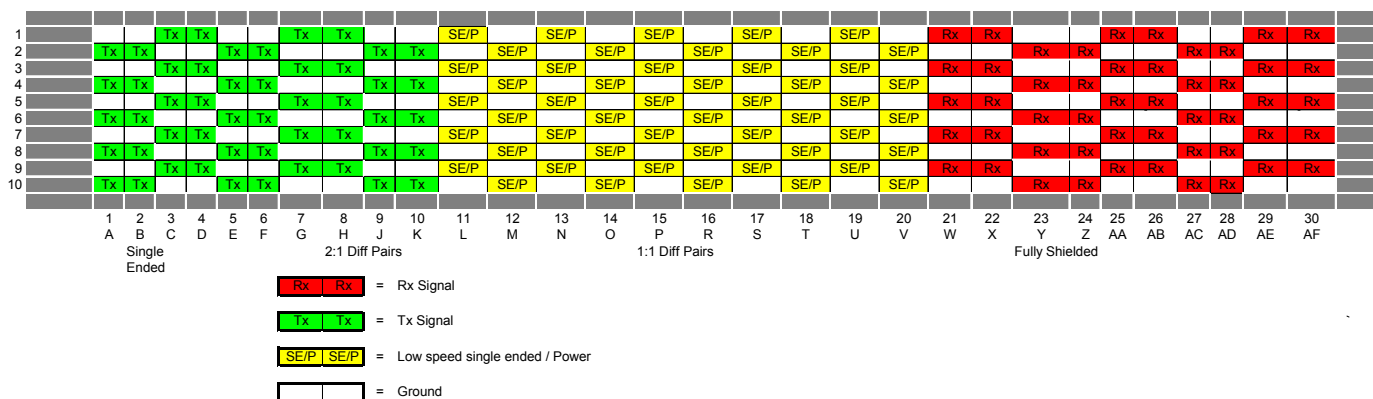


Table A: TX RX grouping separated by low speed (LS) signal columns

REVISION: <b>A</b>	ECR/ECN INFORMATION: EC No: <b>UCP2010-1365</b> DATE: <b>2009/12/01</b>	TITLE: <b>SEARAY BOARD TO BOARD SYSTEM CONNECTOR ROUTING GUIDE</b>	SHEET No. <b>12 of 14</b>
DOCUMENT NUMBER: <b>AS-45970-990</b>	CREATED / REVISED BY: <b>GREGORI</b>	CHECKED BY: <b>SQUIRE / STANCZAK</b>	APPROVED BY: <b>COMERCI</b>

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1			SE/P			SE/P			SE/P			Tx				SE/P			Rx	Rx			Rx	Rx			Rx	Rx		
2	Tx	Tx		Tx	Tx		Tx	Tx		Tx	Tx		Tx	Tx		SE/P	SE/P		Rx	Rx		SE/P		Rx	Rx		SE/P		Rx	Rx
3			SE/P			SE/P			SE/P			Tx				SE/P			Rx	Rx		Rx	Rx		Rx	Rx		Rx	Rx	
4	Tx	Tx		Tx	Tx		Tx	Tx		Tx	Tx		Tx	Tx		SE/P	SE/P		Rx	Rx		SE/P		Rx	Rx		SE/P		Rx	Rx
5			SE/P			SE/P			SE/P			Tx				SE/P			Rx	Rx		Rx	Rx		Rx	Rx		Rx	Rx	
6	Tx	Tx		Tx	Tx		Tx	Tx		Tx	Tx		Tx	Tx		SE/P	SE/P		Rx	Rx		SE/P		Rx	Rx		SE/P		Rx	Rx
7			SE/P			SE/P			SE/P			Tx				SE/P			Rx	Rx		Rx	Rx		Rx	Rx		Rx	Rx	
8	Tx	Tx		Tx	Tx		Tx	Tx		Tx	Tx		Tx	Tx		SE/P	SE/P		Rx	Rx		SE/P		Rx	Rx		SE/P		Rx	Rx
9			SE/P			SE/P			SE/P			Tx				SE/P			Rx	Rx					Rx	Rx				
10	Tx	Tx		Tx	Tx		Tx	Tx		Tx	Tx		Tx	Tx		SE/P	SE/P		Rx	Rx		SE/P		Rx	Rx		SE/P		Rx	Rx

1  
A

2  
B

3  
C

4  
D

5  
E

6  
F

7  
G

8  
H

9  
J

10  
K

11  
L

12  
M

13  
N

14  
O

15  
P

16  
R

17  
S

18  
T

19  
U

20  
V

21  
W

22  
X

23  
Y

24  
Z

25  
AA

26  
AB

27  
AC

28  
AD

29  
AE

30  
AF

Single Ended

2:1 Diff Pairs

1:1 Diff Pairs

Fully Shielded

Rx

Rx

 = Rx Signal

Tx

Tx

 = Tx Signal

SE/P

SE/P

 = Low speed single ended / Power = Ground

Table B: TX RX pairs separated by low speed (LS) signal columns

## Back drilling

For high speed signals, it is highly recommended for any via that extends a significant number of layers below the active signal layer that the excess via stub below the active signal layer is removed by back drilling. In simulation back drilling has shown significant improvement in via impedance and crosstalk. Routing on bottom layer with minimal stub and routing on top layers with control depth via reduces the need for back drilling, but for signals routing on middle layers back drilling is strongly recommended. Since the Searay connector does not require any control of drilling depth to accommodate a press fit or compliant pin, back drilling depth is determined only by the depth of the active layer and the accuracy and resolution of the drilling process.

For a 10mils drill size it is recommended that a 12mils ~14mils drill size be used for back drilling.

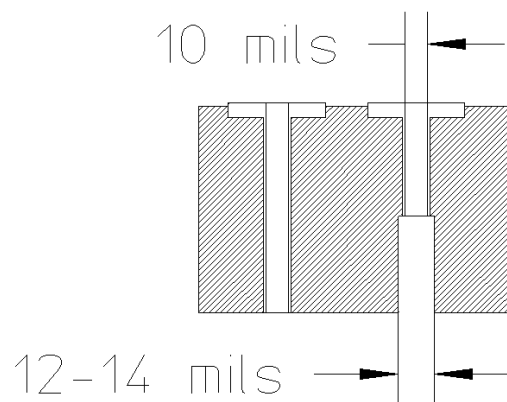


Figure 12: Back Drill Specification

<u>REVISION:</u>  <div style="font-size: 2em; text-align: center;">A</div>	<u>ECR/ECN INFORMATION:</u> <u>EC No:</u> UCP2010-1365 <u>DATE:</u> 2009/12/01	<u>TITLE:</u> <div style="text-align: center; font-weight: bold; font-size: 1.2em;">SEARAY BOARD TO BOARD SYSTEM CONNECTOR ROUTING GUIDE</div>		<u>SHEET No.</u>  <div style="font-size: 1.5em; text-align: center;">13 of 14</div>
<u>DOCUMENT NUMBER:</u> <div style="font-weight: bold; font-size: 1.2em;">AS-45970-990</div>		<u>CREATED / REVISED BY:</u> <div style="text-align: center;">GREGORI</div>	<u>CHECKED BY:</u> <div style="text-align: center;">SQUIRE / STANCZAK</div>	<u>APPROVED BY:</u> <div style="text-align: center;">COMERCI</div>
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# SEARAY CONNECTOR ROUTING GUIDE

## Keep out area

Recommended clearance or keep out area allowed for reworking of this component is .200" (5.0mm) all the way around the perimeter of the part. Contact Molex if further assistance is required.

The required distance between the connector and an impedance discontinuity is highly dependent on the rise time and spectral content of the data transmitted. For a 6.25GHz NRZ differential signal it is recommended that a keep out distance of greater than 12.5mm be kept between the connector and any impedance discontinuity (based on the 1/4 wavelength distance of the clock frequency in the PCB dielectric).

REVISION: <b>A</b>	ECR/ECN INFORMATION: EC No: <b>UCP2010-1365</b> DATE: <b>2009/12/01</b>	TITLE: <b>SEARAY BOARD TO BOARD SYSTEM CONNECTOR ROUTING GUIDE</b>	SHEET No. <b>14 of 14</b>
DOCUMENT NUMBER: <b>AS-45970-990</b>	CREATED / REVISED BY: <b>GREGORI</b>	CHECKED BY: <b>SQUIRE / STANCZAK</b>	APPROVED BY: <b>COMERCI</b>