



FEATURES

- Voltage controlled gain range of 0 dB to 80 dB
- 3 mA supply current at gain of 40 dB
- Low frequency (LF) to 18 MHz operation
- Supply range: 3.0 V to 5.0 V
- Low noise: 4.5 nV/ $\sqrt{\text{Hz}}$ at 80 dB gain
- Fully differential signal path
- Offset correction (offset null) feature
- Internal 1.5 V reference
- 16-lead LFCSP
- Automatic gain control feature
- Wide gain range for high dynamic range signals

APPLICATIONS

- Front end for inductive telemetry systems
- Ultrasonic signal receivers
- Signal compression for driving an ADC
- AGC amplifiers

GENERAL DESCRIPTION

The **AD8338** is a variable gain amplifier (VGA) for applications that require a fully differential signal path, low power, low noise, and a well-defined gain over frequency. While the inputs are differential, the device can also be driven with a single-ended source if required.

The basic gain function is linear-in-dB and is controlled by the voltage applied to Pin GAIN. The nominal gain range spans from 0 dB to 80 dB for control voltages between 0.1 V to 1.1 V with a slope of 12.5 mV/dB. The nominal gain range can be shifted up or down via direct access to Pin INPD and Pin INMD, the current inputs of the VGA. For example, driving the INPD and INMD pins with 50 Ω resistors shifts the gain range up by 20 dB, that is, 20 dB to 100 dB, and lowers the input referred noise of the device to 1.5 nV/ $\sqrt{\text{Hz}}$. Additionally, the gain slope can be inverted via logic Pin MODE.

The **AD8338** includes additional circuit blocks to enable input offset correction and automatic gain control (AGC). DC offset voltages are removed by the offset correction circuit, which behaves like a high-pass filter whose corner is set with an external capacitor. The AGC function varies the gain of the **AD8338** to maintain a constant RMS output voltage. An externally applied voltage to Pin VAGC with respect to the voltage at Pin VREF sets the output RMS amplitude. A capacitor from Pin DETO to ground sets the response time of the AGC circuit.

FUNCTIONAL BLOCK DIAGRAM

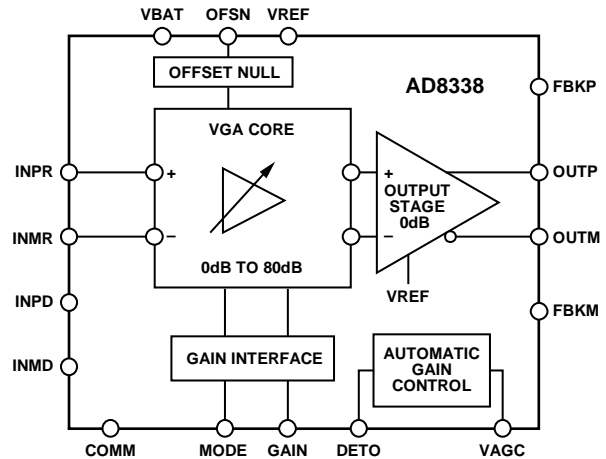


Figure 1.

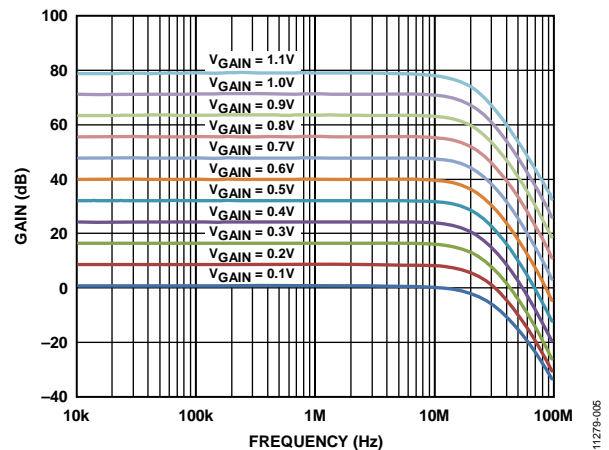


Figure 2. Gain vs. Frequency

The **AD8338** offers additional versatility by providing access to the internal summing nodes of the VGA core and the output amplifiers. With the addition of a few external passive components, users can customize the gain, bandwidth, input impedance, and noise profile of the part to fit their application.

The **AD8338** uses a single supply voltage of 3.0 V to 5.0 V and is very power efficient, consuming as little as 3 mA quiescent current at mid gain. The **AD8338** is available in a 3 mm \times 3 mm, RoHS compliant, 16-lead LFCSP and is specified over the industrial temperature range of -40°C to $+85^{\circ}\text{C}$.

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REVISION HISTORY

11/13—Rev. 0 to Rev. A

| | |
|---|----|
| Changes to Features Section, Applications Section, and General Descriptions Section | 1 |
| Changes to Table 1 | 3 |
| Changes to Pin 13 and Pin 14 Descriptions | 5 |
| Added Conditions to Typical Performance Characteristics; Changes to Figure 4 and Figure 5; Changes to Figure 6, Figure 7, Figure 8 Captions | 6 |
| Changes to Figure 12 and Figure 13 | 7 |
| Changes to Figure 18 and Figure 19 | 8 |
| Changes to Figure 22 | 9 |
| Changes to Figure 35 and Figure 36 | 11 |
| Replaced Theory of Operation Section | 12 |
| Changes to Figure 50 | 18 |
| Changes to Ordering Guide | 20 |

4/13—Revision 0: Initial Version

SPECIFICATIONS

AC SPECIFICATIONS

$V_{BAT} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 2\text{ pF}$ on OUTP and OUTM, $R_L = \infty$, MODE pin high, $R_{IN} = 2 \times 500\ \Omega$, $V_{GAIN} = 0.6\text{ V}$, differential operation, unless otherwise noted.

Table 1.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|--------------------------------------|---|------|----------|-----------|------------------------|
| INPUT INTERFACE | | | | | |
| Input Voltage Range | INPD, INMD, INPR, INMR pins | | 3 | | V p-p |
| –3 dB Bandwidth | | | 18 | | MHz |
| Input Resistance | Standard configuration using the INPR and INMR inputs | 0.8 | 1 | 1.2 | k Ω |
| Input Capacitance | | | 2 | | pF |
| OUTPUT INTERFACE | | | | | |
| Small Signal Bandwidth | OUTP and OUTM pins $V_{GAIN} = 0.6\text{ V}$ | | 18 | | MHz |
| Peak Slew Rate | $V_{GAIN} = 0.6\text{ V}$ | | 50 | | V/ μs |
| Peak-to-Peak Output Swing | Differential output | | 2.8 | | V p-p |
| Common-Mode Voltage | | | 1.5 | | V |
| Input-Referred Voltage Noise | | | | | |
| Using Internal Resistors | $V_{GAIN} = 1.1\text{ V}$ | | 4.5 | | nV/ $\sqrt{\text{Hz}}$ |
| | $V_{GAIN} = 0.6\text{ V}$ | | 15 | | nV/ $\sqrt{\text{Hz}}$ |
| | $V_{GAIN} = 0.1\text{ V}$ | | 150 | | nV/ $\sqrt{\text{Hz}}$ |
| Using External 47 Ω Resistors | $V_{GAIN} = 1.1\text{ V}$ | | 1.5 | | nV/ $\sqrt{\text{Hz}}$ |
| Offset Voltage | RTO, $V_{GAIN} = 0.1\text{ V}$, offset null enabled | –10 | | +10 | mV |
| | RTO, $V_{GAIN} = 0.6\text{ V}$, offset null enabled | –10 | | +10 | mV |
| | RTO, $V_{GAIN} = 0.1\text{ V}$, offset null disabled | –50 | | +50 | mV |
| | RTO, $V_{GAIN} = 0.6\text{ V}$, offset null disabled | –200 | | +200 | mV |
| POWER SUPPLY | | | | | |
| V_{BAT} | | 3.0 | | 5.0 | V |
| I_{VBAT} | Min gain, $V_{GAIN} = 0.1\text{ V}$ | | 6.0 | 8.0 | mA |
| | Mid gain, $V_{GAIN} = 0.6\text{ V}$ | | 3.0 | 3.8 | mA |
| | Max gain, $V_{GAIN} = 1.1\text{ V}$ | | 4.5 | 6.0 | mA |
| GAIN CONTROL | | | | | |
| Gain Range | Standard configuration using the INPR and INMR inputs | 0 | | 80 | dB |
| Gain Span | | | 80 | | dB |
| Gain Voltage | V_{GAIN} relative to COMM | 0.1 | | 1.1 | V |
| Gain Slope | | 77 | 80 | 83 | dB/V |
| | | 12 | 12.5 | 13 | mV/dB |
| Gain Accuracy | Standard configuration using the INPR and INMR inputs; $0.1\text{ V} < V_{GAIN} < 1.1\text{ V}$ | –2 | +0.5 | +2 | dB |
| VREF REFERENCE OUTPUT | | | | | |
| Output Voltage | | | 1.5 | | V |
| Output Current | | | 5 | | mA |
| Accuracy | | | 2 | | % |
| DETO OUTPUT CURRENT | | | | | |
| | | | ± 10 | | μA |
| MODE INPUT | | | | | |
| Logic High | | 2.5 | | V_{BAT} | V |
| Logic Low | | COMM | | 0.6 | V |
| AGC CONTROL | | | | | |
| Maximum Target Amplitude | MODE = 0 V Expected rms output value for target = $V_{AGC} - V_{REF} = 1.0\text{ V}$ | | 1.0 | | V rms |

ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter | Rating |
|--|------------------|
| VBAT to COMM | −0.3 V to +5.5 V |
| INPR, INPD, INMD, INMR, MODE, GAIN, FBKM, FBKP, OUTM, OUTP, VAGC, VREF, OFSN | COMM to VBAT |
| Operating Temperature Range | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Maximum Junction Temperature | 150°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 3. Thermal Resistance

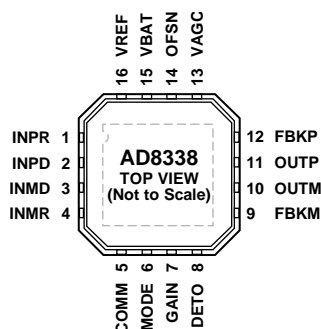
| Package Type | θ_{JA} | Unit |
|---------------|---------------|------|
| 16-Lead LFCSP | 48.75 | °C/W |

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD SHOULD BE TIED TO A QUIET ANALOG GROUND.

11279-002

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|----------|--|
| 0 | EPAD | Exposed Pad. The exposed pad should be tied to a quiet analog ground. |
| 1 | INPR | Positive 500 Ω Resistor Input for Voltage Input Applications. |
| 2 | INPD | Positive Input for Current Input Applications. |
| 3 | INMD | Negative Input for Current Input Applications. |
| 4 | INMR | Negative 500 Ω Resistor Input for Voltage Input Applications. |
| 5 | COMM | Ground. |
| 6 | MODE | Gain Mode. This pin selects positive or negative gain slope for gain control. When this pin is tied to VBAT, the gain of the AD8338 increases proportionally with an increase of the voltage on the GAIN pin. When this pin is tied to COMM, the gain decreases with an increase of the voltage on the GAIN pin. |
| 7 | GAIN | Gain Control Input, 12.5 mV/dB or 80 dB/V. |
| 8 | DETO | Detector Output Terminal, $\pm 10 \mu\text{A}$. If the AGC feature is not used, tie DETO to COMM. |
| 9 | FBKM | Negative Feedback Node. For more information, see the FBKP, FBKM, OUTP, and OUTM Pins section. |
| 10 | OUTM | Negative Output. |
| 11 | OUTP | Positive Output. |
| 12 | FBKP | Positive Feedback Node. For more information, see the FBKP, FBKM, OUTP, and OUTM Pins section. |
| 13 | VAGC | Voltage for Automatic Gain Control Circuit. This pin controls the target rms output voltage for the AGC circuit. For more information, see the AGC Circuit, VAGC Pin section. If the AGC feature is not used, tie VAGC to VREF. |
| 14 | OFSN | Offset Null Terminal. For more information, see the Offset Correction Circuit, OFSN Pin section. If the offset null feature is not used, tie OFSN to ground; otherwise, a capacitor to VREF is used to set the offset null high-pass corner. |
| 15 | VBAT | Positive Supply Voltage. |
| 16 | VREF | Internal 1.5 V Voltage Reference. |

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{BAT} = 3.0\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 2\text{ pF}$ on OUTP and OUTM, $R_L = \infty$, MODE pin high, $R_{IN} = 2 \times 500\ \Omega$, $V_{GAIN} = 0.6\text{ V}$, differential operation; unless otherwise noted.

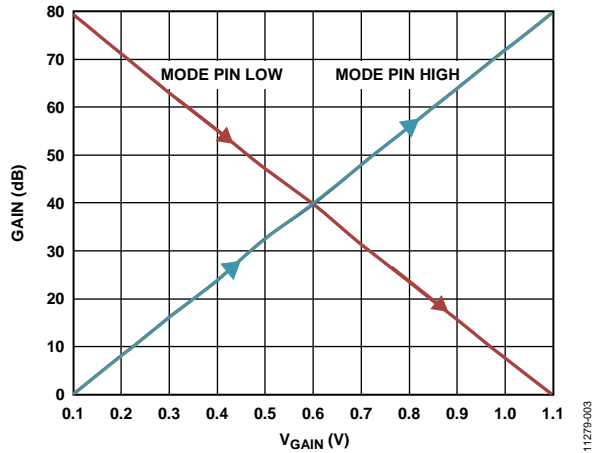


Figure 4. Gain vs. V_{GAIN}

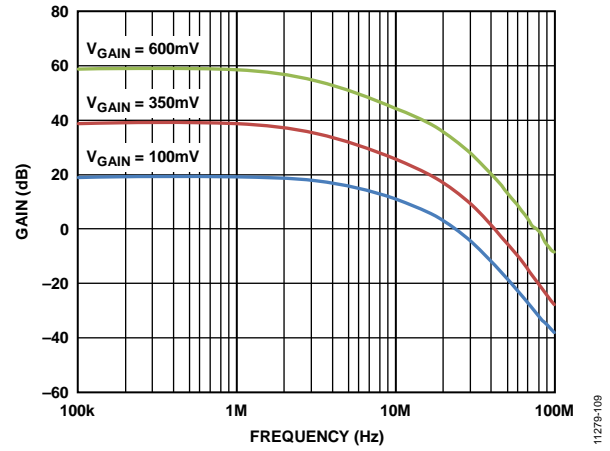


Figure 7. Gain vs. Frequency, $R_{IN} = 50\ \Omega$, 20 dB Steps

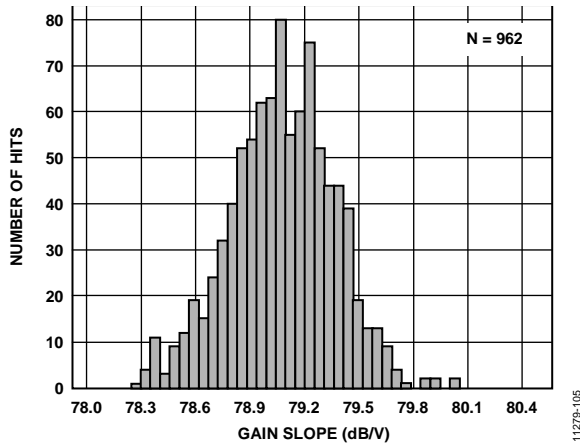


Figure 5. Gain Slope Histogram

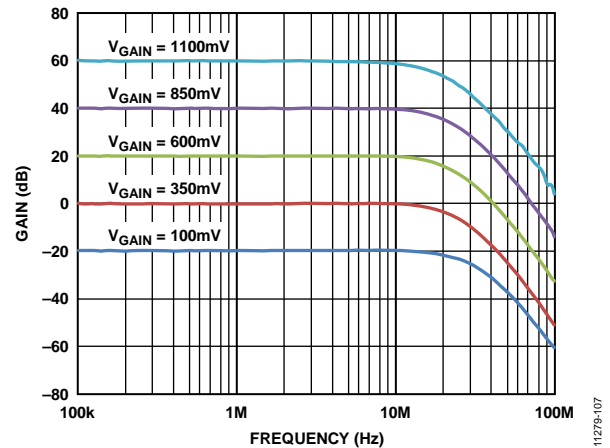


Figure 8. Gain vs. Frequency, $R_{IN} = 5\text{ k}\Omega$, 20 dB Steps

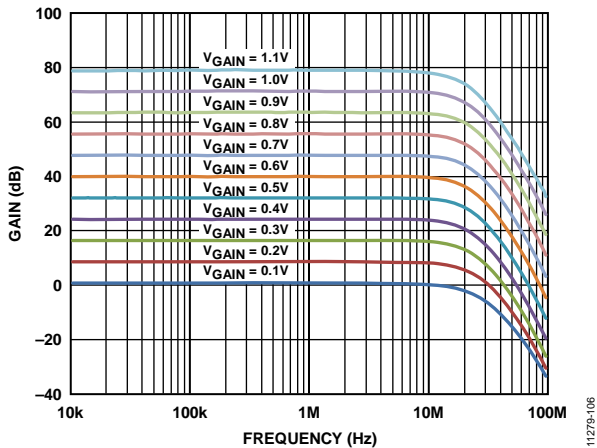


Figure 6. Gain vs. Frequency, 8 dB Steps

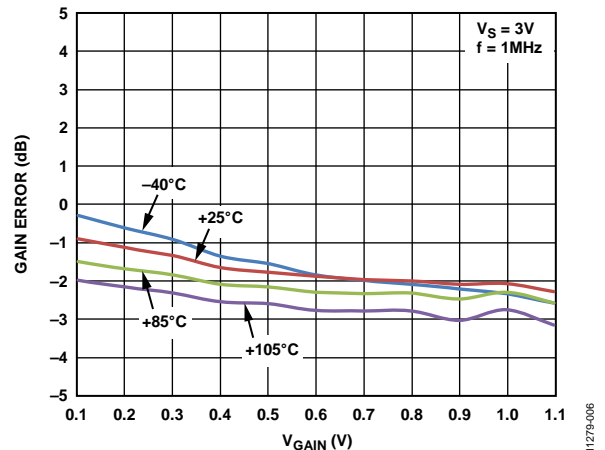


Figure 9. Gain Error vs. V_{GAIN} over Temperature

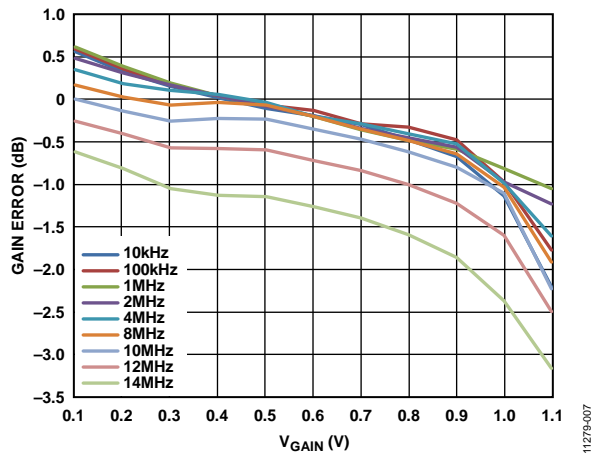
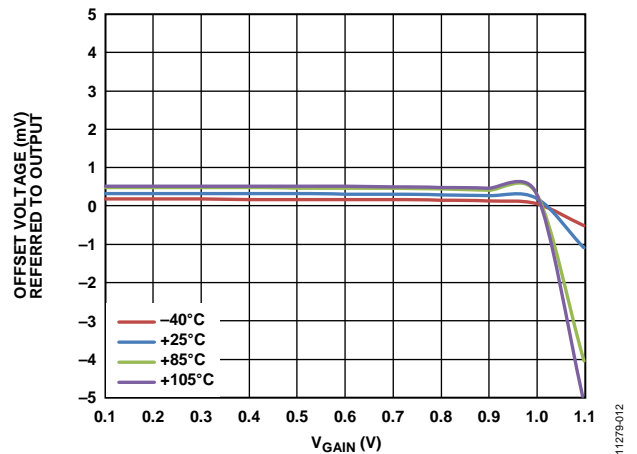
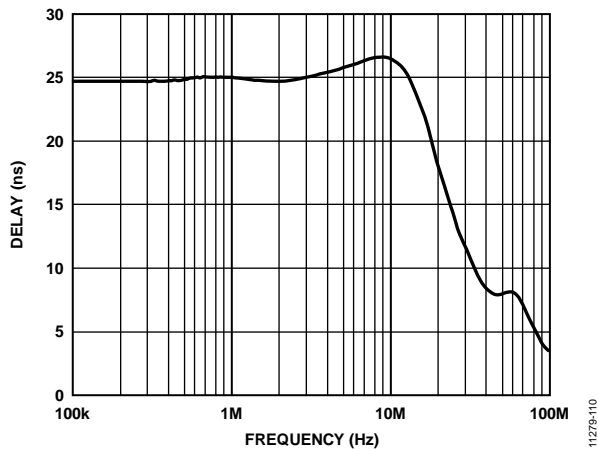
Figure 10. Gain Error vs. V_{GAIN} over FrequencyFigure 13. Differential Offset Voltage vs. V_{GAIN} , Offset Null On

Figure 11. Group Delay vs. Frequency

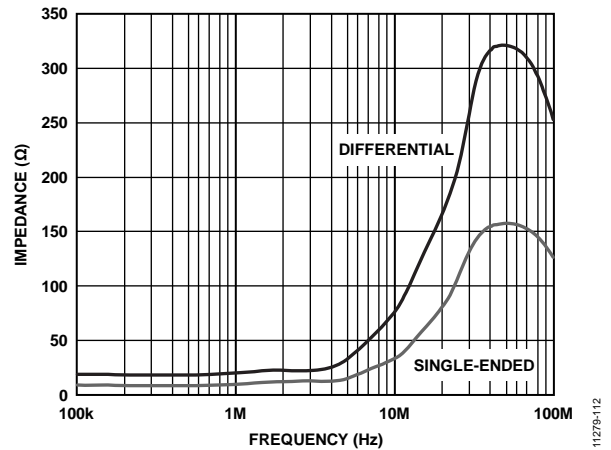


Figure 14. Output Impedance vs. Frequency

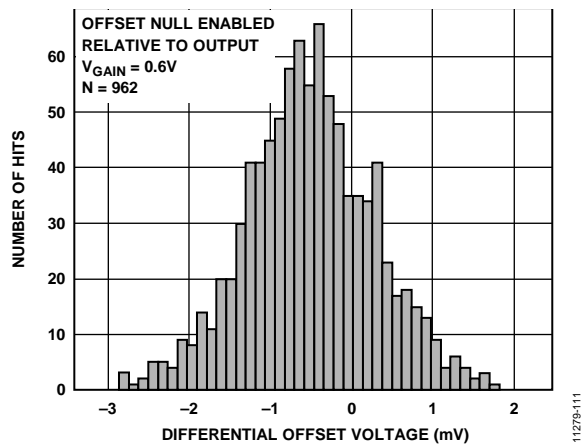


Figure 12. Differential Offset Voltage Histogram

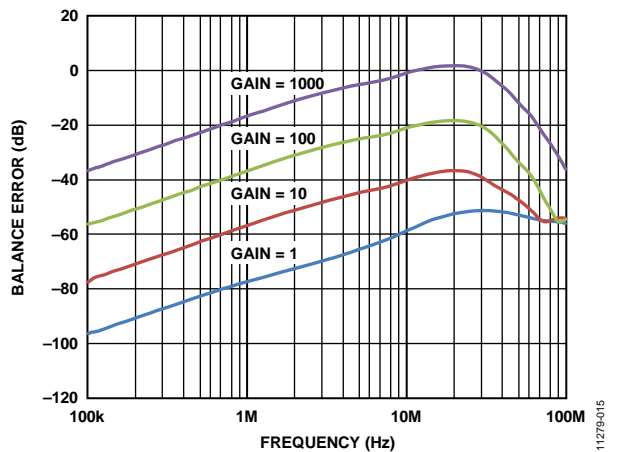


Figure 15. Output Balance Error vs. Frequency

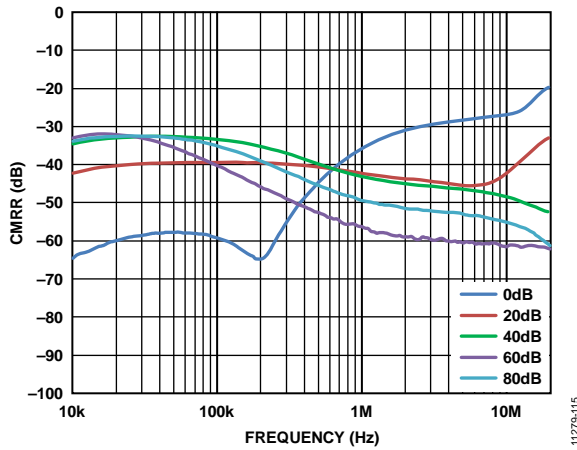


Figure 16. CMRR vs. Frequency over Gain, Offset Null On, Referred to Input

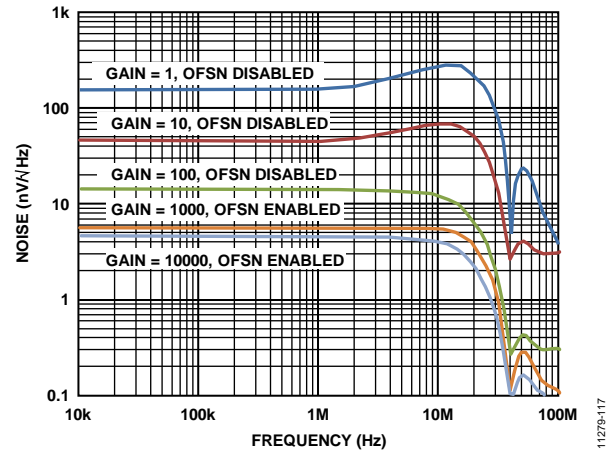


Figure 19. Input Referred Noise vs. Frequency

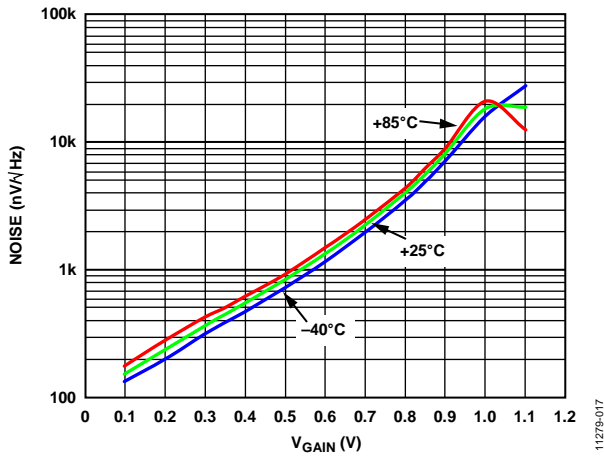


Figure 17. Output Referred Noise vs. V_{GAIN}

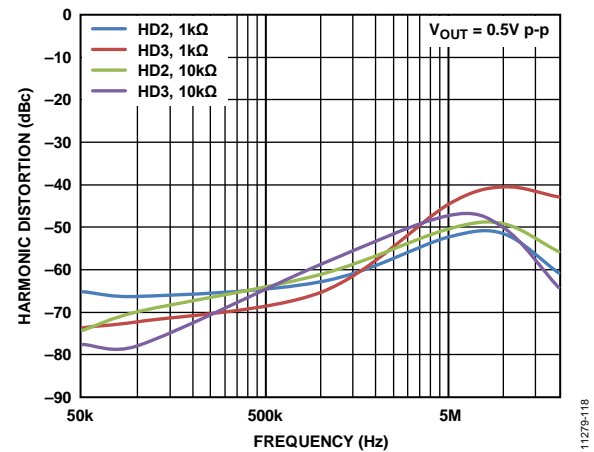


Figure 20. Harmonic Distortion vs. Frequency

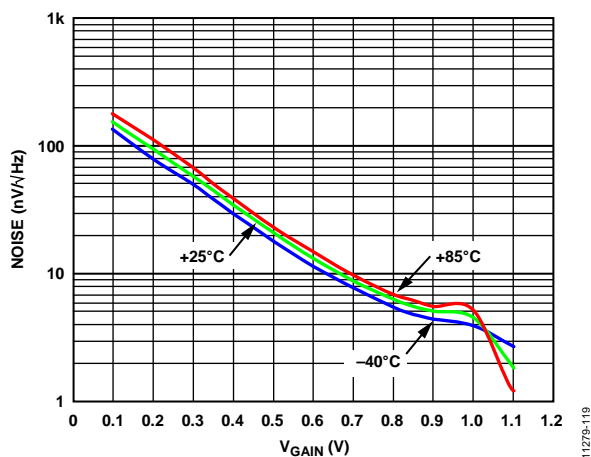


Figure 18. Input Referred Noise vs. V_{GAIN}

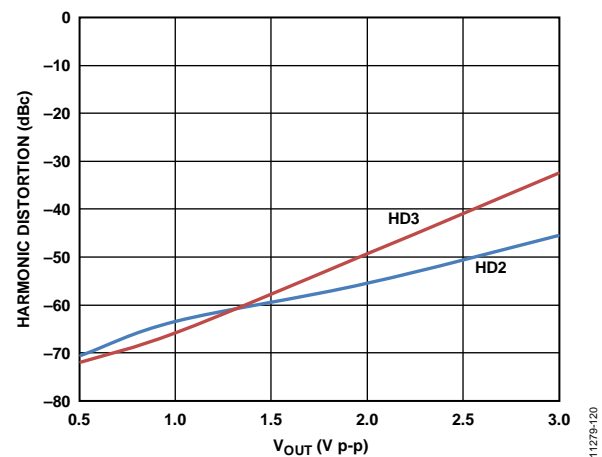


Figure 21. Harmonic Distortion vs. Output Amplitude

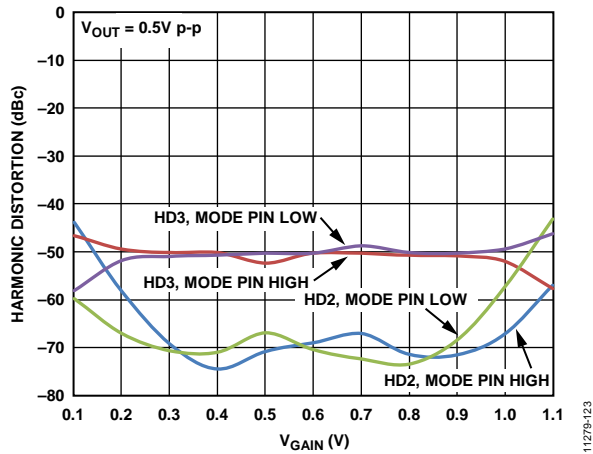
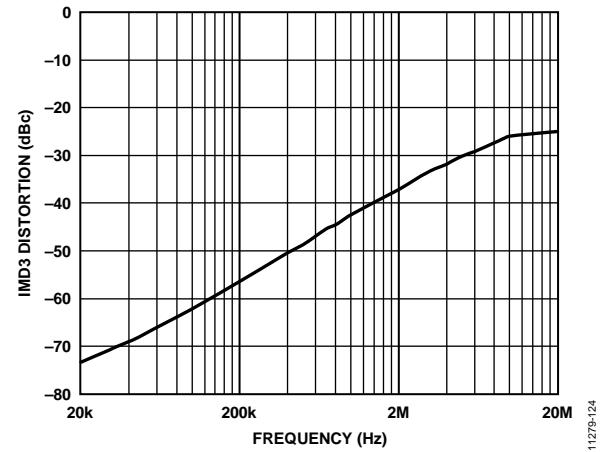
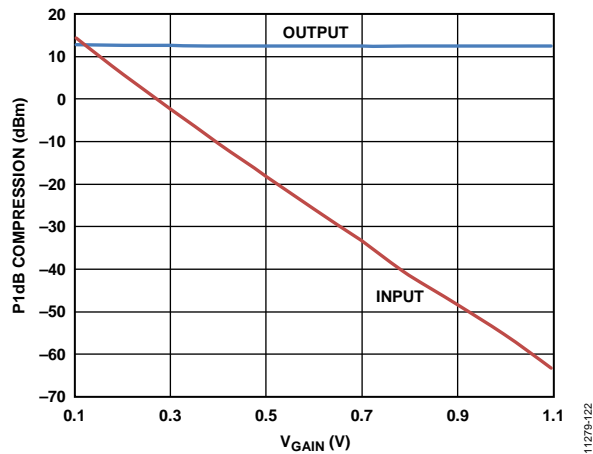
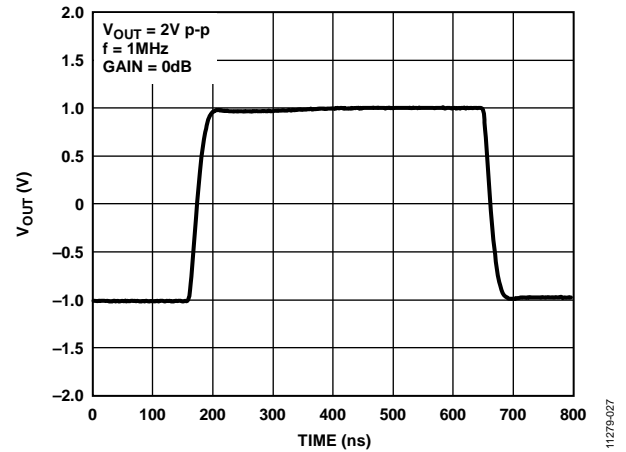
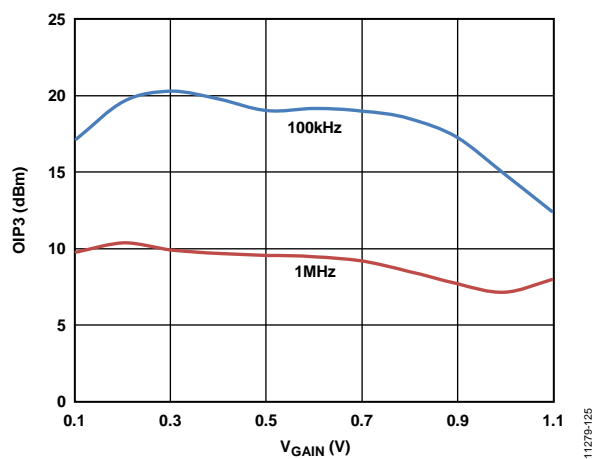
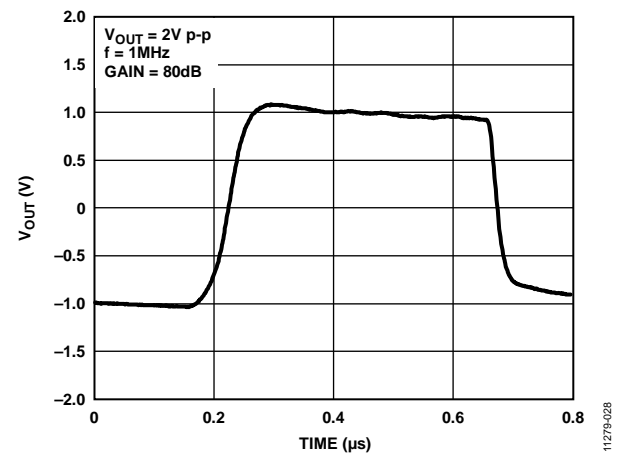
Figure 22. Harmonic Distortion vs. V_{GAIN} 

Figure 25. IMD3 Distortion vs. Frequency

Figure 23. Input and Output 1 dB Compression vs. V_{GAIN} Figure 26. Large Signal Pulse Response vs. Time, $V_{GAIN} = 0\text{ V}$ Figure 24. OIP3 vs. V_{GAIN} Figure 27. Large Signal Pulse Response vs. Time, $V_{GAIN} = 1.0\text{ V}$

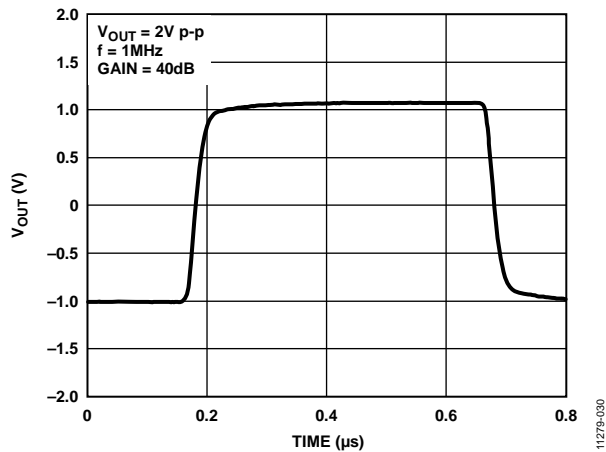
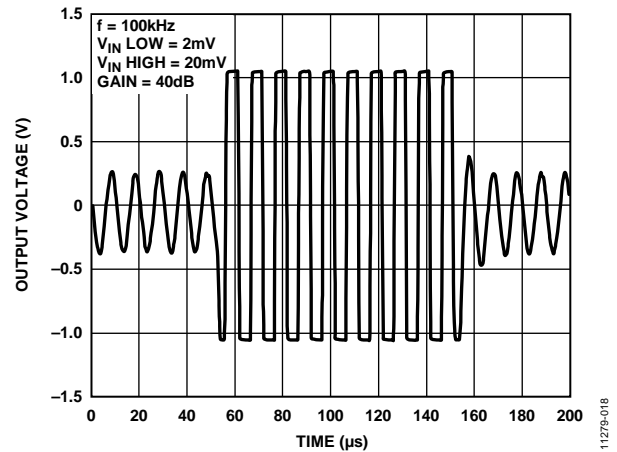
Figure 28. Large Signal Pulse Response vs. Time, $V_{GAIN} = 0.6V$ 

Figure 31. Overdrive Recovery vs. Time

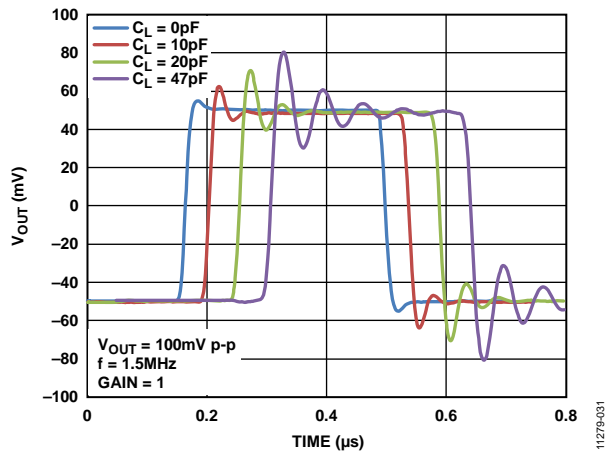


Figure 29. Small Signal Pulse Response vs. Time (Varying Capacitive Loads)

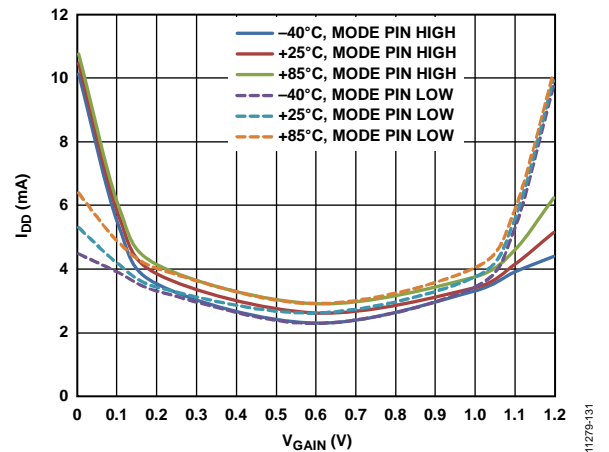
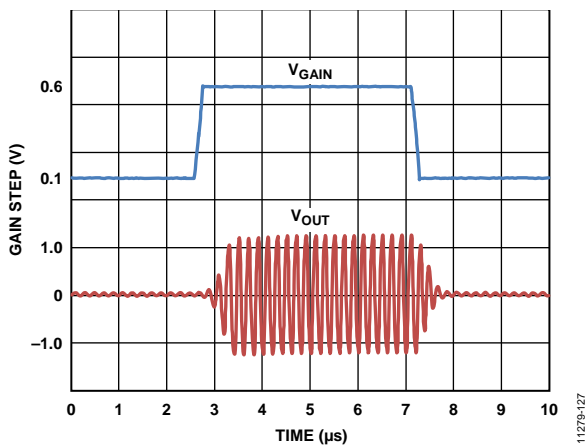
Figure 32. Supply Current vs. V_{GAIN} 

Figure 30. Gain Step Response vs. Time

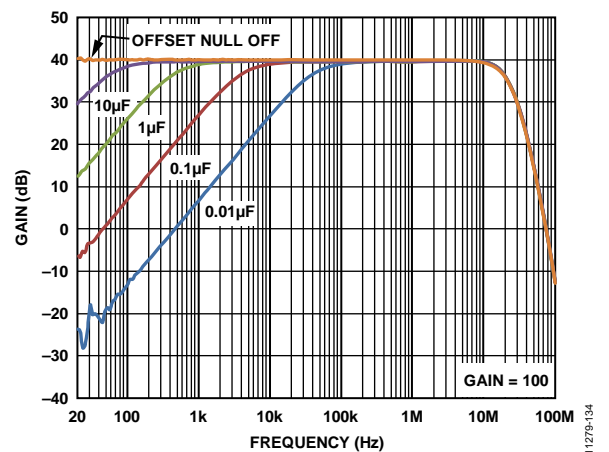


Figure 33. Offset Null Bandwidth vs. Offset Null Capacitor

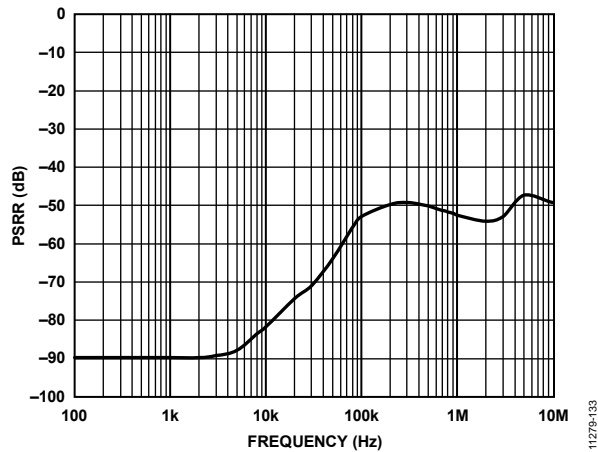
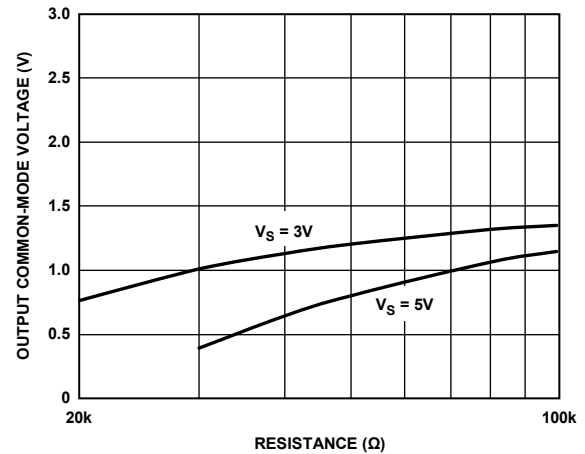


Figure 34. PSRR vs. Frequency

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Figure 37. Output Common-Mode Voltage vs. R_{CM} to VBAT

11279-135

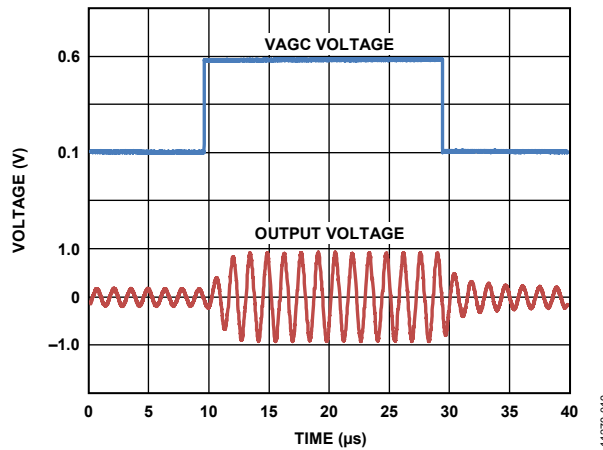
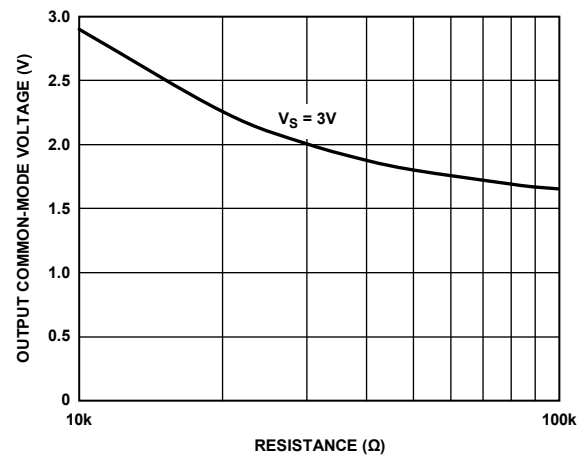
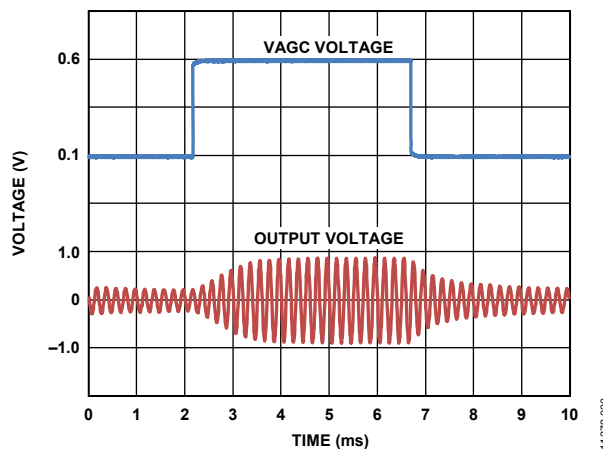


Figure 35. AGC Response vs. Time, No Load, Input 100 mV Differential

11279-019

Figure 38. Output Common-Mode Voltage vs. R_{CM} to COMM

11279-136

Figure 36. AGC Response vs. Time, $C_L = 0.01 \mu F$, Input 100 mV Differential

11279-020

THEORY OF OPERATION

INTRODUCTION

The AD8338 is a single supply variable gain amplifier (VGA) with an adjustable gain range of 80 dB. More accurately, the AD8338 is an input variable gain amplifier (IVGA), which has been designed to accept a wide range of input amplitudes, and via its variable gain, compress it to either a narrow range of output amplitudes or a constant output amplitude (for example, automatic gain control applications). Like other VGAs from Analog Devices, Inc., the AD8338 possesses a constant bandwidth over the entire gain range. Therefore, with a bandwidth of 18 MHz, the AD8338 achieves a gain-bandwidth product of 180 GHz at its highest gain setting (gain of 80 dB). Additionally, the differential output of the AD8338 allows the VGA to directly drive differential input ADCs without the need of a single-ended-to-differential converter.

OVERALL STRUCTURE OF THE AD8338

Figure 39 shows a block schematic of the AD8338 depicting the key sections of the VGA and a general overview of its features. The AD8338 signal path is comprised by the 500 Ω input resistors, the VGA core, and the transimpedance output amplifiers. The gain of the signal path is adjusted by the linear-in-dB gain interface and the voltage at Pin GAIN with respect to its local ground, Pin COMM. The automatic gain control (AGC) circuit block, is a current output RMS detector that can be used to drive the GAIN pin and configure the AD8338 as an AGC amplifier with constant RMS output amplitude. This output amplitude is adjusted by the voltage at Pin VAGC with respect to the voltage at Pin VREF. The offset null circuit block allows the AD8338 to auto zero any dc offset voltages. To enable the offset null functionality, connect a capacitor between the OFSN and VREF pins. To disable the offset null functionality, connect Pin OFSN to ground. The INPD, INMD, FBKP, and FBKM pins provide access to internal nodes in the VGA core of the AD8338 and output amplifiers allowing the user to adjust the gain range, output common-mode voltage, and bandwidth of the device.

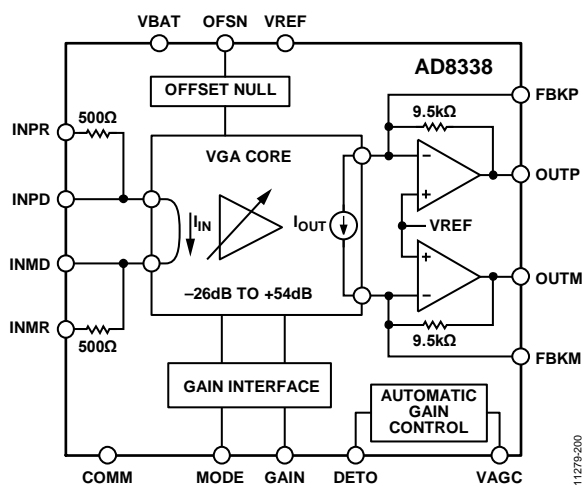


Figure 39. Block Schematic

VGA CORE

Figure 40 shows a simplified diagram of the VGA core at the heart of the AD8338. The key concepts regarding the operation of this VGA core are as follows: First, the ratio of the collector currents in the two differential pairs (Q1, Q2 and Q3, Q4) is identical given that the two differential pairs share the same base drive. This ratio is represented by the modulation factor, x , where values of x range from -1 and $+1$. Second, the input current signal is forced into the collectors of the input differential pair (Q1, Q2) by means of the loop amplifier to modulate the fixed tail current, I_D , and set the modulation factor, x . The value of x in the input differential pair is replicated to the output differential pair (Q3, Q4) to modulate its fixed tail current, I_N , and generate a differential output current. Third, the current gain of this cell is exactly $G = I_N/I_D$ over many decades of variable bias current.

By varying I_N , the overall function of the cell is that of a two-quadrant analog multiplier, exhibiting a linear relationship to both the signal modulation factor, x , and this numerator current. On the other hand, by varying I_D , the overall function is that of a two-quadrant analog divider, having a hyperbolic gain function with respect to the modulation factor, x , controlled by this denominator current. Because the AD8338 is an input VGA, it controls I_D to adjust the amplifier's gain. However, because a hyperbolic gain function is generally of less value than one in which the decibel gain is a linear function of a control input, the AD8338 includes a special interface to provide either increasing or decreasing exponential control of I_D .

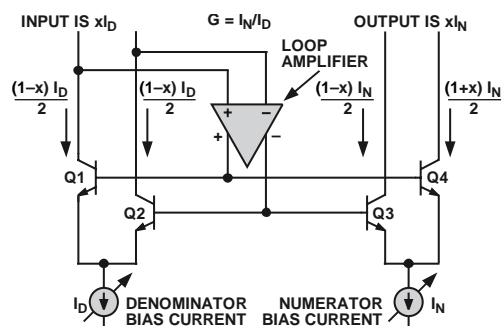


Figure 40. Simplified Diagram of the VGA Core

NORMAL OPERATING CONDITIONS

Normal operating conditions for the AD8338 are defined as follows:

- The input pins, INPR and INMR, are voltage driven (the source impedance is assumed to be zero).
- The output pins, OUTP and OUTM, are open circuited (the load impedance is assumed to be infinite).
- Pin COMM is grounded.
- Pin MODE is either tied to a logic high or left unconnected, to set the noninverted gain slope gain mode.

INPR, INMR, INPD, and INMD Pins

The input signal to the AD8338 is accepted at the INPR/INMR and the INPD/INMD differential input ports. These pins are internally biased to approximately 1.5 V, the voltage at reference Pin VREF. The INPR and INMR pins are voltage input pins (see Figure 41) where the differential input voltage and the internal input resistors generate current, I_{IN} , the input current for the VGA core. While the voltage inputs can be driven in either a single-sided or a differential manner, operation using a differential drive is preferable, and is assumed in all specifications, unless otherwise stated. The pin-to-pin input resistance between the voltage inputs is specified as $1000\ \Omega \pm 20\%$. In most cases, the voltage input pins are ac-coupled via two capacitors chosen to provide adequate low frequency transmission. This results in the minimum input noise that increases when a common-mode voltage other than 1.5 V is forced onto these input pins. The short-circuit (INPR shorted to INMR) input-referred noise at maximum gain is approximately $4.5\ \text{nV}/\sqrt{\text{Hz}}$.

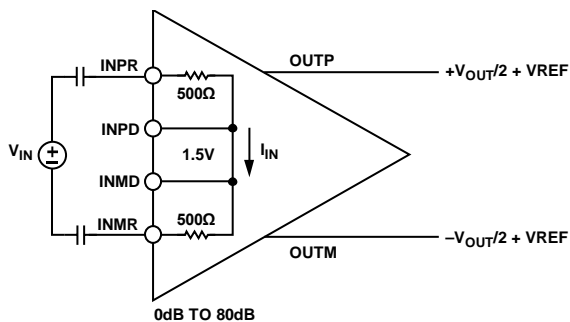


Figure 41. Input Voltage Applied to the INPR and INMR Pins

The INPD and INMD pins are current input pins (see Figure 42) where the differential input current is directly applied to the VGA core input. This input current can either be generated with an external current source like an unbiased photodiode, or with a voltage source and external coupling resistors (see Figure 43). The latter method allows the gain range of the AD8338 to be shifted as explained in the Explanation of the Gain Function section. When using the INPD and INMD inputs, the INPR and INMR pins should be shorted to one another to prevent stability issues.

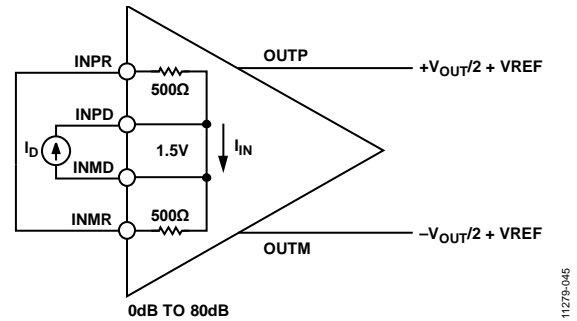


Figure 42. Input Current Applied to the INPD and INMD Pins

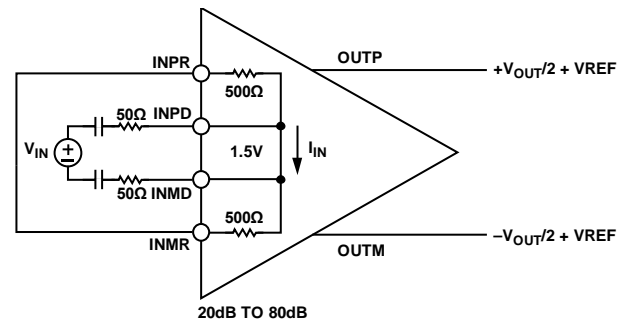


Figure 43. Using External Resistors at the INPD and INMD Pins

FBKP, FBKM, OUTP, and OUTM Pins

Output voltage pins, OUTP and OUTM, have a default common-mode voltage of 1.5 V, the voltage at the VREF reference pin. This output common-mode voltage can be adjusted by injecting common-mode currents into Pin FBKP and Pin FBKM, the summing nodes of the output amplifiers, which are also biased at 1.5 V. The output amplifiers of the AD8338 possess rail-to-rail output stages which allow the output common mode of the VGA to be shifted from ground to the positive supply, though the use of such extreme values leaves only a small range for the differential output signal swing.

Adding feedback capacitors, C_{FBK} , across nodes (OUTP, FBKP and OUTM, FBKM) reduces bandwidth of the output amplifiers of the AD8338 and the signal path of the VGA. These capacitors and the feedback resistors of the output amplifiers form a low-pass filter with a cut-off frequency of approximately:

$$f_c = \frac{1}{2\pi \times R_{FBK} \times C_{FBK}} \quad (1)$$

where R_{FBK} are the internal feedback resistors of the output amplifiers. R_{FBK} is specified as $9800\ \Omega \pm 20\%$.

Reducing the bandwidth of the AD8338 minimizes output noise and simplifies the design of the antialiasing filter when using the VGA to drive an ADC.

Linear-in-dB Gain Control, GAIN Pin

To facilitate the use of an 80 dB gain range, the AD8338 has a linear-in-dB gain control. The gain is controlled by the voltage at Pin GAIN with respect to the local ground COMM. In normal operating conditions, adjusting the voltage at Pin GAIN from 0.1 V to 1.1 V adjusts the gain from its lowest value of 0 dB to its highest value of 80 dB. The basic gain equation is

$$G(\text{dB}) = \frac{V_{\text{GAIN}}}{12.5 \text{ mV}} - 8 \text{ dB} \quad (2)$$

where V_{GAIN} is in volts.

Alternatively, the gain equation can be expressed as a numerical gain magnitude

$$G_N = 0.398 \times 10^{\frac{V_{\text{GAIN}}}{250 \text{ mV}}} \quad (3)$$

where V_{GAIN} is in volts.

Inversion of the Gain Slope, MODE Pin

Pin MODE controls the polarity of the gain adjustment. That is, Pin MODE allows the slope of the gain function to be inverted. If Pin MODE is tied to VBAT, the gain of the AD8338 increases exponentially (or linear-in-dB) with an increase in the voltage at Pin GAIN. If Pin MODE is tied to COMM, the gain of the AD8338 decreases exponentially (or linear-in-dB) with an increase in the voltage at Pin GAIN. Figure 44 shows the two gain control modes when the AD8338 is configured in normal operating conditions.

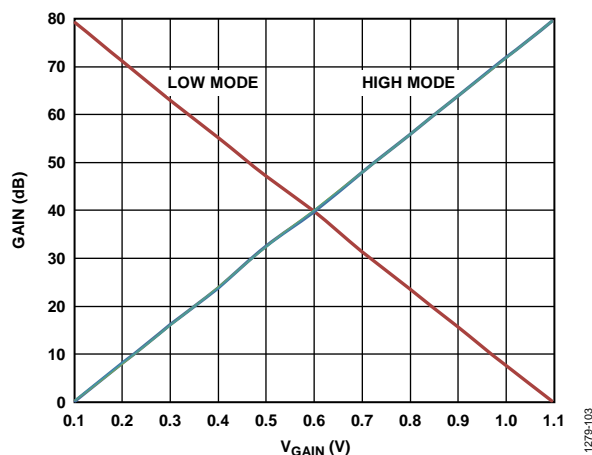


Figure 44. Two Gain Control Modes of the AD8338

Offset Correction Circuit, OFSN Pin

The AD8338 includes an internal offset correction circuit that cancels out any dc offsets that may be present in the VGA. Connecting a capacitor, C_{OFSN} , between Pin OFSN and Pin VREF enables the offset correction circuit.

The offset correction circuit uses an internal autozero feedback loop, which introduces small signal high-pass filter characteristics to the signal path. The -3 dB corner frequency is

$$f_{\text{OFSN}} = \frac{1}{2\pi \times 400 \Omega \times C_{\text{OFSN}}} \quad (4)$$

Even though the AD8338 exhibits a high-pass filter characteristic in its transfer function when the offset correction circuit is enabled, the latter should not be used as a high-pass filter due to the narrow voltage range of dc input voltages the circuit can reject. If signals at frequencies below the band of interest need to be rejected, for best performance, incorporate a high-pass filter preceding the AD8338. This can be achieved by ac-coupling the inputs as shown in Figure 41.

To provide a dc-coupled signal path, the offset correction circuit can be disabled by connecting Pin OFSN to Pin COMM. Exercise caution when operating the AD8338 with the offset correction circuit disabled, because at large gains, dc offsets will cause large dc errors at the outputs of the VGA.

AGC Circuit, VAGC Pin

The AD8338 includes a current output RMS detector that can be used to configure the AD8338 as an AGC amplifier (see Figure 46).

In this configuration, the AGC circuit compares the RMS output amplitude of the VGA with the desired RMS output amplitude (voltage at Pin VAGC with respect to the voltage at Pin VREF), and drives Pin GAIN to minimize their difference. Therefore, in steady state conditions, the circuit forces the RMS output amplitude of the AD8338 to be the voltage at Pin VAGC with respect to the voltage at Pin VREF. Because the AGC circuit uses negative feedback, the gain slope of the AD8338 needs to be inverted by connecting Pin MODE to ground.

The bandwidth of the AGC circuit is dictated by Capacitor C_{DETO} . Choose this capacitor carefully to ensure that the bandwidth of the AGC circuit is high enough so that it can react to fast changes in the input signal's amplitude, but low enough to prevent the AGC circuit from distorting the signal of interest. For example, in an on-off keying (OOK) application with a carrier frequency of 6.8 MHz and a bit rate of 10 kb/s, it is recommended to use a 0.01 μF capacitor. This capacitor value ensures that the gain reacts to the bit energy but does not react to the carrier signal.

As mentioned previously, the AGC circuit forces the RMS output amplitude of the AD8338 to be the voltage at Pin VAGC with respect to the voltage at Pin VREF. Furthermore, the input to the AGC circuit, Pin VAGC, is symmetrical with respect to Pin VREF. In other words, the AGC circuit responds to the

absolute value of the difference in voltage between Pin VAGC and Pin VREF (see Figure 45).

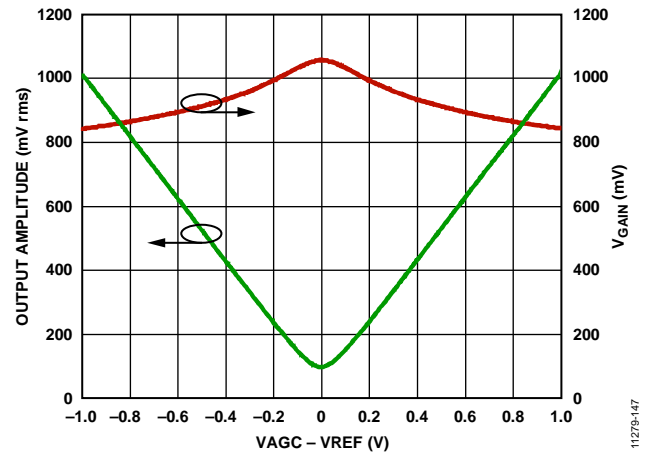


Figure 45. Output RMS Voltage and VGAIN vs. VAGC – VREF

Not all applications require the AGC circuit. Therefore, the AGC circuit can be disabled by connecting Pin DETO to ground, and connecting Pin VAGC to Pin VREF.

Internal Reference, Pin VREF

The AD8338 includes an internal 1.5 V voltage reference that is used to set the quiescent bias voltages of many key nodes in the VGA. These nodes include inputs pins (INPR, INMR, INPD, and INMD), output pins (OUTP and OUTM), and feedback pins (FKBP and FBKM). The output voltage of the internal reference, Pin VREF, may be bypassed with a 0.1 μF capacitor to Pin COMM, but do not force it externally.

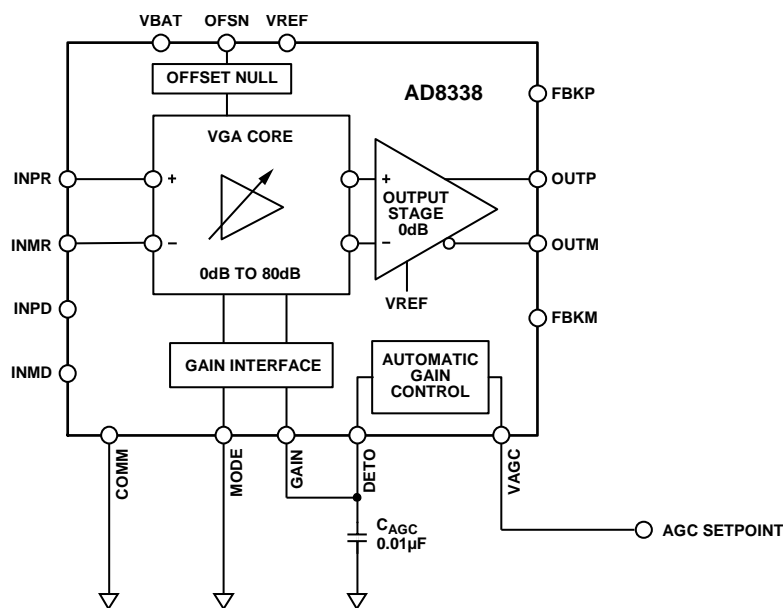


Figure 46. AD8338 Configured as an AGC Amplifier

EXPLANATION OF THE GAIN FUNCTION

The signal chain of the [AD8338](#) can be broken down into three stages. The first stage is a differential voltage-to-current converter comprised by the input resistors, R_P and R_N , of the VGA. These input resistors may either be the internal 500 Ω resistors coupled to Pin INPR and Pin INMR, or external resistors coupled to Pin INPD and Pin INMD. The trans-resistance of the voltage-to-current converter is $R_P + R_N$ such that the current flowing in the resistors is given by:

$$I_{IN} = \frac{V_{INPx} - V_{INMx}}{R_P + R_N} \quad (5)$$

The current in the input resistors, I_{IN} , is fed to the second stage of the [AD8338](#), the VGA core. The VGA core is a fully differential variable gain current amplifier with a gain range of 80 dB. In the noninverting gain slope setting (Pin MODE connected to Pin VBAT), the current gain of the VGA core spans from -26 dB ($V_{GAIN} = 0.1$ V) to +54 dB ($V_{GAIN} = 1.1$ V). In numerical gain magnitude, the gain of the VGA core is given by

$$I_{OUT,VGA} = I_{IN} \times 10^{(80 V_{GAIN} - 34)/20} \approx I_{IN} \times 0.02 \times 10^{\frac{V_{GAIN}}{250 \text{ mV}}} \quad (6)$$

The differential output current of the VGA core is fed to the third stage of the [AD8338](#), a fully differential current-to-voltage converter comprised by the output amplifiers and their corresponding feedback resistors, R_{FBK} . The overall transimpedance of the current to voltage converter is $2R_{FBK}$, such that the differential output voltage of the stage is given by:

$$V_{OUT,DIFF} = I_{OUT,VGA} \times 2 \times R_{FBK} \quad (7)$$

Therefore, the overall voltage gain of the [AD8338](#) is:

$$G(\text{dB}) = 80 \times V_{GAIN} \times 20 \times \log\left(\frac{2 \times R_{FBK}}{R_P + R_N}\right) - 34 \quad (8)$$

Alternatively, the gain equation can be expressed as a numerical gain magnitude,

$$G_N = 0.02 \times \frac{2 \times R_{FBK}}{R_P + R_N} \times 10^{\frac{V_{GAIN}}{250 \text{ mV}}} \quad (9)$$

Equation 8 and Equation 9 show that the gain range of the [AD8338](#) can be shifted by using external input resistors, R_P and R_N . For example, driving the INPD and INMD pins with an R_P and R_N of 50 Ω shifts the gain range of the [AD8338](#) up by 20 dB, from 20 dB to 100 dB (see Figure 43). Similarly, driving the INPD and INMD pins with an R_P and R_N of 5 k Ω , shifts the gain range down by 20 dB, from -20 dB to +60 dB.

As shown in Figure 43, when using external resistors to drive the INPD and INMD pins, short the INPR and INMR pins to one another to prevent stability issues.

Effects of Using External Resistors

When the gain range is shifted through the use of external resistors, several trade-offs must be considered. External resistors connected to Pin INPD and Pin INMD load the current inputs of the VGA core changing the dynamic behavior of the block and the -3 dB bandwidth of the [AD8338](#). The -3 dB bandwidth of the [AD8338](#) with external resistors is

$$f_{CL} = 18 \text{ MHz} \times \left(\frac{500 \Omega \times R_{EXT}}{500 \Omega + R_{EXT}} \right) \times \frac{1}{500 \Omega} \quad (10)$$

For example, with 50 Ω external resistors, the input-referred noise at maximum gain decreases to approximately 1 nV/ $\sqrt{\text{Hz}}$ and the gain range shifts up by 20 dB. However, the -3 dB bandwidth is reduced from 18 MHz to approximately 1.8 MHz.

ADJUSTING THE OUTPUT COMMON-MODE VOLTAGE

The output common-mode voltage of the AD8338 differential outputs is nominally set to 1.5 V, the voltage at Pin VREF. This output common-mode voltage can be adjusted by connecting a resistor from each of the output amplifier's summing nodes (Pin FBKP and Pin FBKM) to either Pin COMM or Pin VBAT. Connecting a resistor from Pin FBKP and Pin FBKM to Pin VBAT decreases the output common-mode voltage, whereas connecting a resistor from Pin FBKP and Pin FBKM to Pin COMM increases the output common-mode voltage (see Figure 47 and Figure 48).

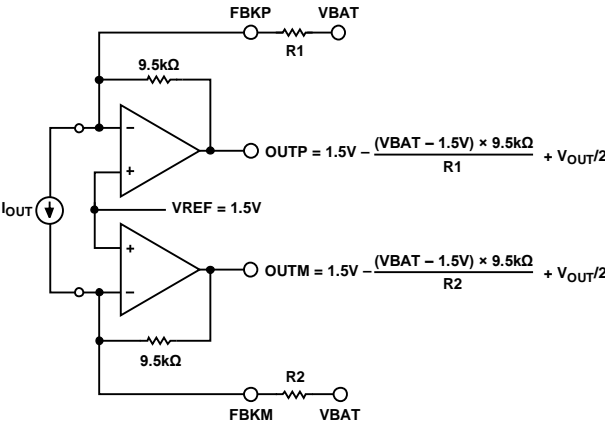


Figure 47. Decreasing the Output Common-Mode Voltage

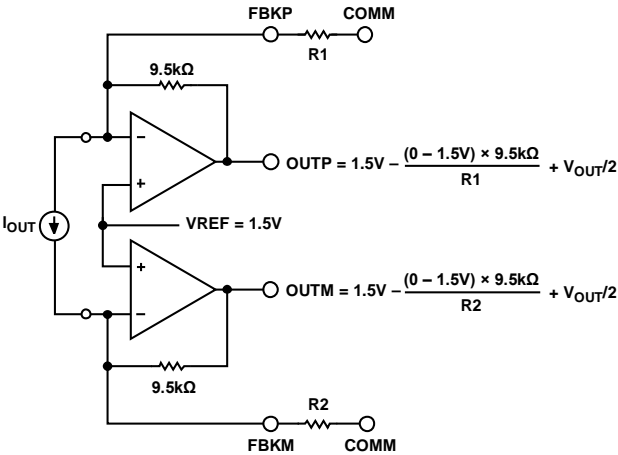


Figure 48. Increasing the Output Common-Mode Voltage

Table 5 and Table 6 show suggested values for the external resistors shown in Figure 47 and Figure 48.

Table 5. Resistor Values for Decreasing the Output Common-Mode Voltage

| VBAT (V) | Target V _{OCM} (V) | Resistor Value (Ω) | Tied to |
|----------|-----------------------------|--------------------|---------|
| 5.0 | 0.9 | 55,417 | VBAT |
| 3.3 | 0.9 | 28,500 | VBAT |
| 3.0 | 0.9 | 23,750 | VBAT |

Table 6. Resistor Values for Increasing the Output Common-Mode Voltage

| VBAT (V) | Target V _{OCM} (V) | Resistor Value (Ω) | Tied to |
|----------|-----------------------------|--------------------|---------|
| Any | 1.8 | 47,500 | COMM |
| Any | 2.0 | 28,500 | COMM |
| Any | 2.5 | 14,250 | COMM |

APPLICATIONS INFORMATION

The excellent performance of the AD8338 results in a flat response over various gains with rail-to-rail output signal swing, high drive capability, and a very high dynamic range at a low 12 mW. These features make the AD8338 an exceptional choice for use in battery-operated equipment, low frequency and baseband applications, and many other applications.

SIMPLE ON-OFF KEYED (OOK) RECEIVER

For low complexity, low power data communications, a simple link built using a modulating carrier tone in an on/off state provides a fast and cost-effective solution to the designer. Such designs are used in a variety of applications, including near-field communications among noninterference mechanical systems, low data rate sensors, RFID tags, and so on.

The schematic shown in Figure 49 demonstrates a complete inductive telemetry on-off keyed (OOK) front end. The crystal is cut for the target receive frequency of interest, creating a very narrow-band filter, typically around the 6.78 MHz ISM band.

The AD8338 amplifies the signal (the gain is set by an external controller) and drives a full-wave rectifier bridge. The output of this bridge is then low-pass filtered into 100 Ω terminations. This design provides excellent rejection of RF and excellent baseband information recovery for the decision stage that follows.

The reactive filter components—Capacitors C1 through C4 and Inductors L1 and L2—set the baseband recovery performance. A design trade-off exchanges baseband response for RF attenuation.

Table 7 provides typical values for these components at two data rates. Note that Capacitors C1 through C4 are all of equal value, and Inductor L2 has the same value as L1.

| Table 7. Typical Values for Components in Reactive Filter | | | |
|---|----------|-----------|------------------------------------|
| Data Rate | C1 to C4 | L1 and L2 | Carrier Attenuation (f = 6.78 MHz) |
| 19,200 bps | 12 nF | 240 μH | −101 dB |
| 57,600 bps | 3.9 nF | 82 μH | −73 dB |

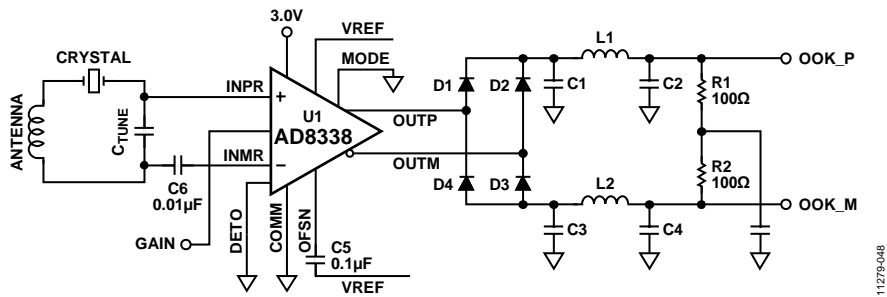
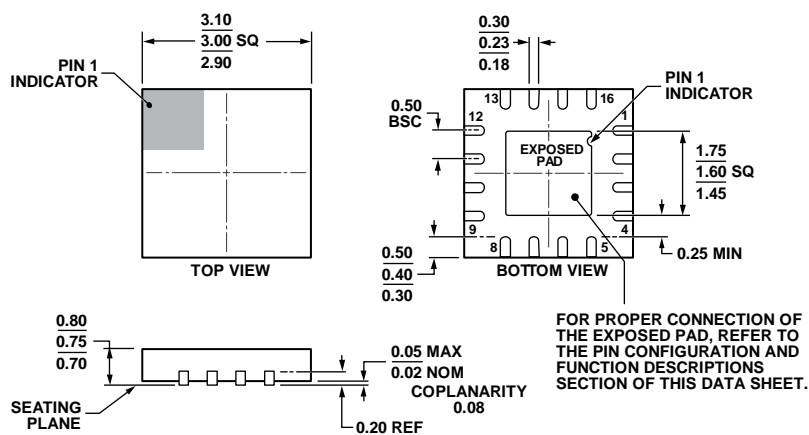


Figure 49. Complete, Low Power OOK Receiver

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 51. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
 3 mm × 3 mm Body, Very Very Thin Quad
 (CP-16-22)
 Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option | Branding |
|--------------------|-------------------|--|----------------|----------|
| AD8338ACPZ-R7 | −40°C to +85°C | 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-16-22 | Y4K |
| AD8338ACPZ-RL | −40°C to +85°C | 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-16-22 | Y4K |
| AD8338-EVALZ | | AD8338 Evaluation Board | | |

¹ Z = RoHS Compliant Part.