

N-Channel 75-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
75	0.011 at $V_{GS} = 10$ V	28	33 nC
	0.0145 at $V_{GS} = 4.5$ V	28	

FEATURES

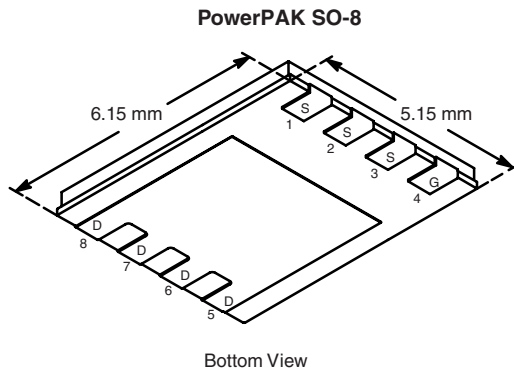
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET
- 100 % R_g Tested



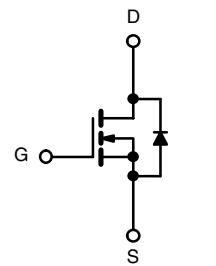
RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Primary Side Switch



Ordering Information: Si7148DP-T1-E3 (Lead (Pb)-free)
Si7148DP-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	75	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	28	A
	$T_C = 70^\circ\text{C}$	22	
	$T_A = 25^\circ\text{C}$	28 ^{b, c}	
	$T_A = 70^\circ\text{C}$	12 ^{b, c}	
Pulsed Drain Current	I_{DM}	60	A
Continuous Source-Drain Diode Current	$T_C = 25^\circ\text{C}$	28	
	$T_A = 25^\circ\text{C}$	4.3 ^{b, c}	
Avalanche Current	$L = 0.1$ mH	45	mJ
Single-Pulse Avalanche Energy		100	
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	96	W
	$T_C = 70^\circ\text{C}$	61	
	$T_A = 25^\circ\text{C}$	5.4 ^{b, c}	
	$T_A = 70^\circ\text{C}$	3.4 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

Notes:

a. Based on $T_C = 25^\circ\text{C}$.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 10$ s.

d. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	18	23	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.0	1.3	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. Maximum under Steady State conditions is 65 °C/W.

SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = 250$ μ A	75			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250$ μ A		75		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ μ A	1.5	2.0	2.5	V
		$V_{DS} = V_{GS}$, $I_D = 5$ mA		2.3		
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 75$ V, $V_{GS} = 0$ V			1	μ A
		$V_{DS} = 75$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 10$ V	30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 15$ A		0.0091	0.011	Ω
		$V_{GS} = 4.5$ V, $I_D = 13.5$ A		0.012	0.0145	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15$ V, $I_D = 15$ A		60		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 35$ V, $V_{GS} = 0$ V, $f = 1$ MHz		2900		pF
Output Capacitance	C_{oss}			370		
Reverse Transfer Capacitance	C_{rss}			196		
Total Gate Charge	Q_g	$V_{DS} = 38$ V, $V_{GS} = 10$ V, $I_D = 15$ A		68	100	nC
		$V_{DS} = 38$ V, $V_{GS} = 4.5$ V, $I_D = 15$ A		33	50	
Gate-Source Charge	Q_{gs}			9.5		
Gate-Drain Charge	Q_{gd}			16.8		
Gate Resistance	R_g	$f = 1$ MHz	0.5	1.1	1.7	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 38$ V, $R_L = 3.8$ Ω $I_D \cong 10$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ Ω		33	50	ns
Rise Time	t_r			255	390	
Turn-Off Delay Time	$t_{d(off)}$			35	55	
Fall Time	t_f			100	150	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 38$ V, $R_L = 3.8$ Ω $I_D \cong 10$ A, $V_{GEN} = 10$ V, $R_g = 1$ Ω		17	26	
Rise Time	t_r			46	70	
Turn-Off Delay Time	$t_{d(off)}$			39	60	
Fall Time	t_f			18	30	

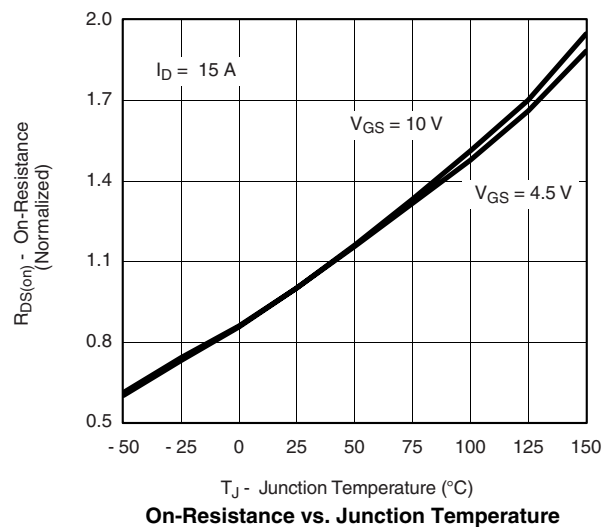
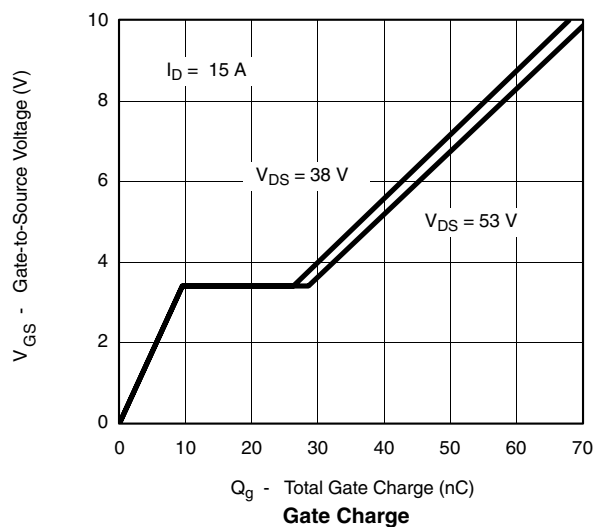
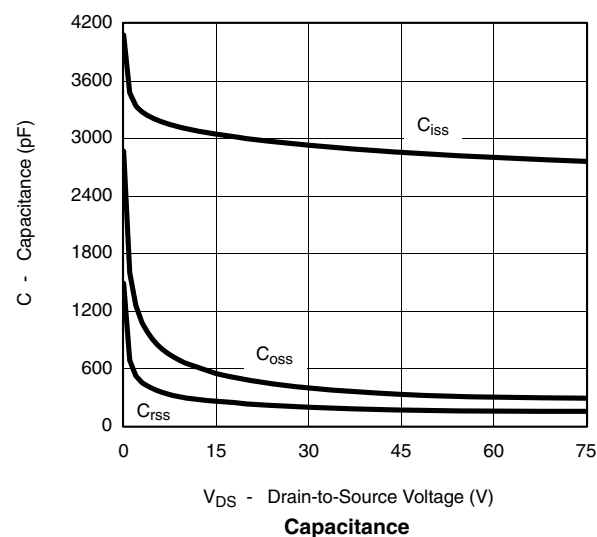
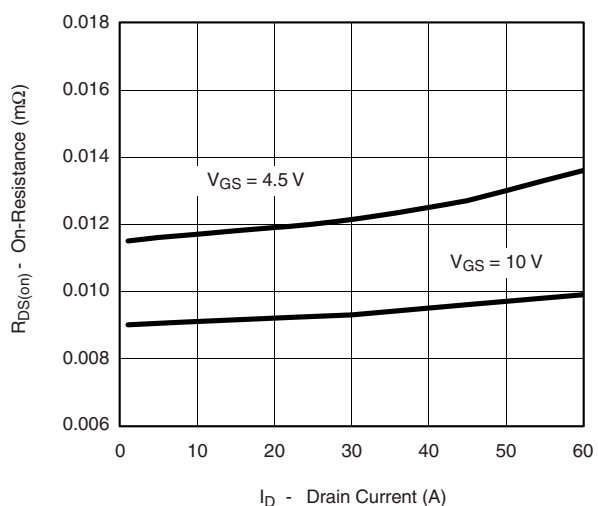
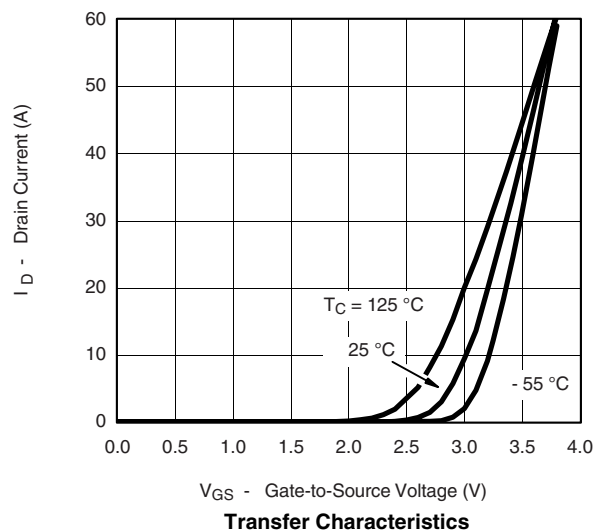
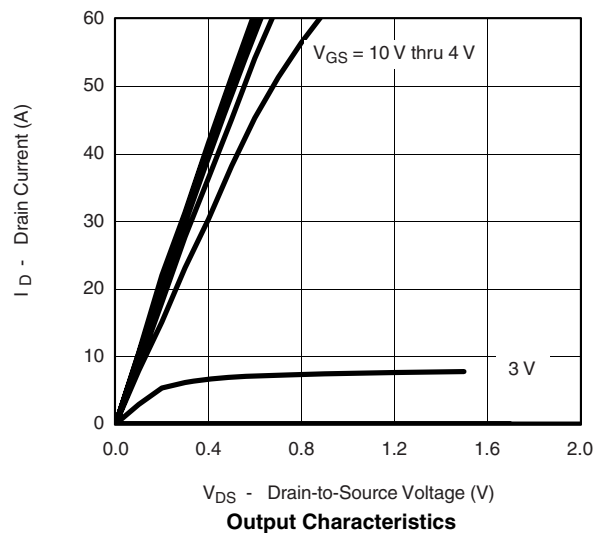


SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$			25	A
Pulse Diode Forward Current ^a	I_{SM}				60	
Body Diode Voltage	V_{SD}	$I_S = 4.3\text{ A}$		0.76	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 12\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$		41	65	ns
Body Diode Reverse Recovery Charge	Q_{rr}			67	105	nC
Reverse Recovery Fall Time	t_a			27		ns
Reverse Recovery Rise Time	t_b			14		

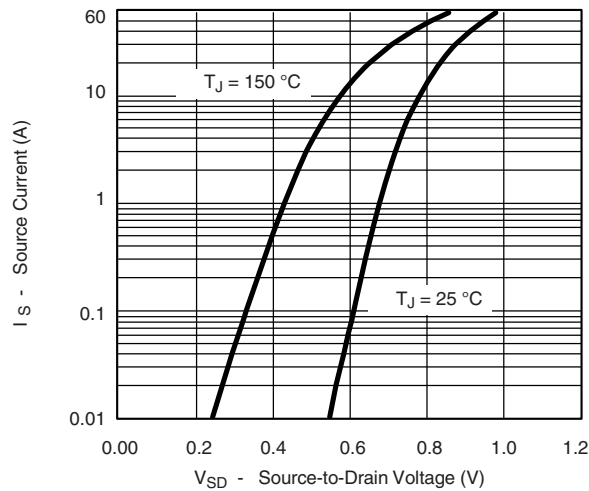
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

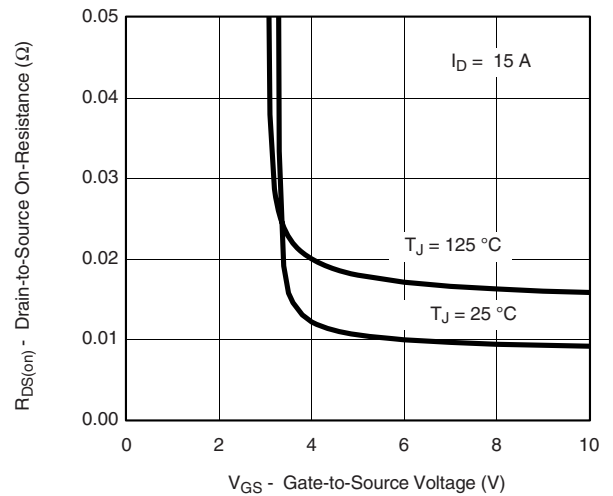
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

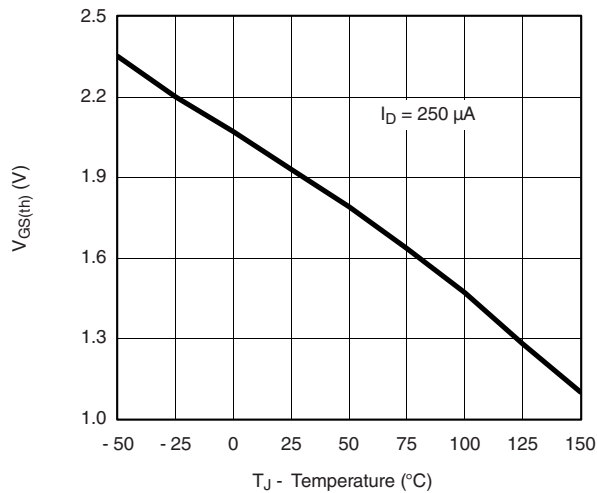
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



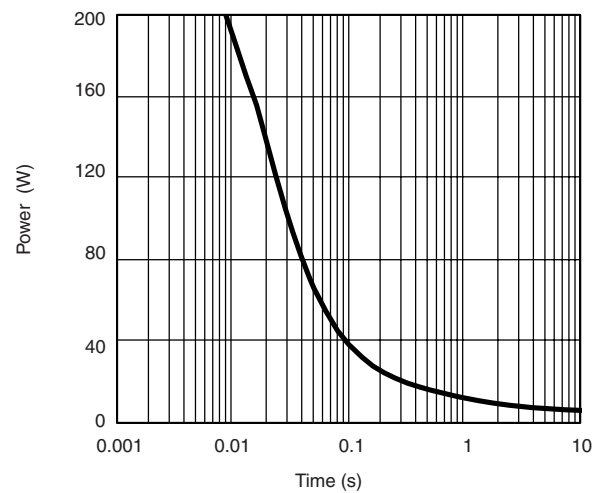
Source-Drain Diode Forward Voltage



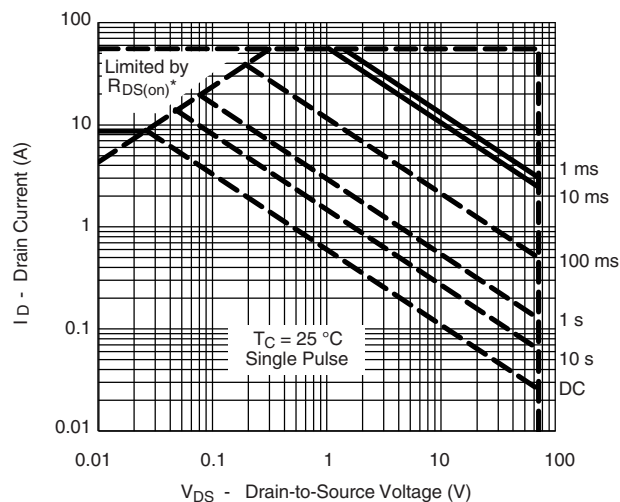
On-Resistance vs. Gate-to-Source Voltage



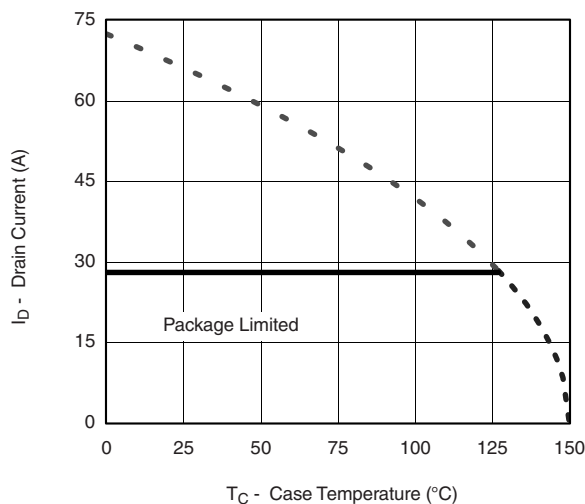
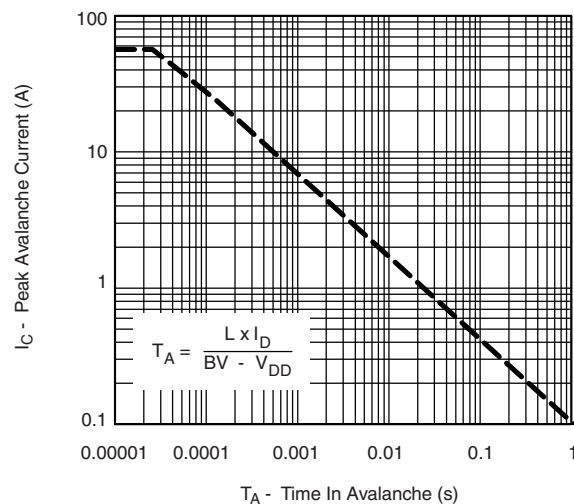
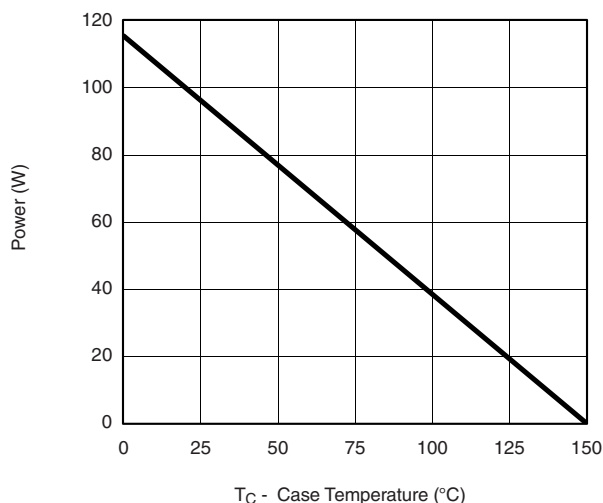
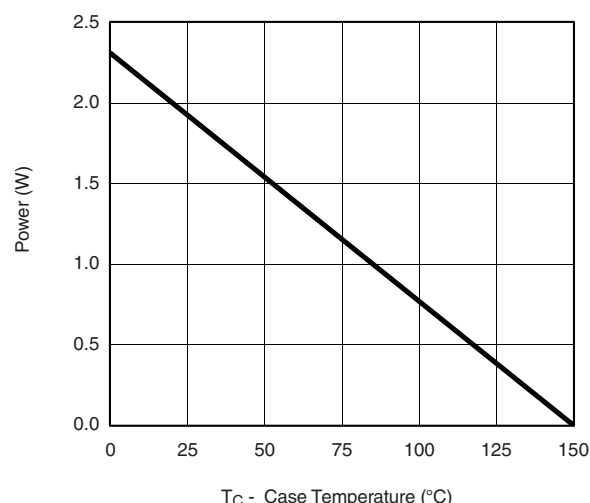
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

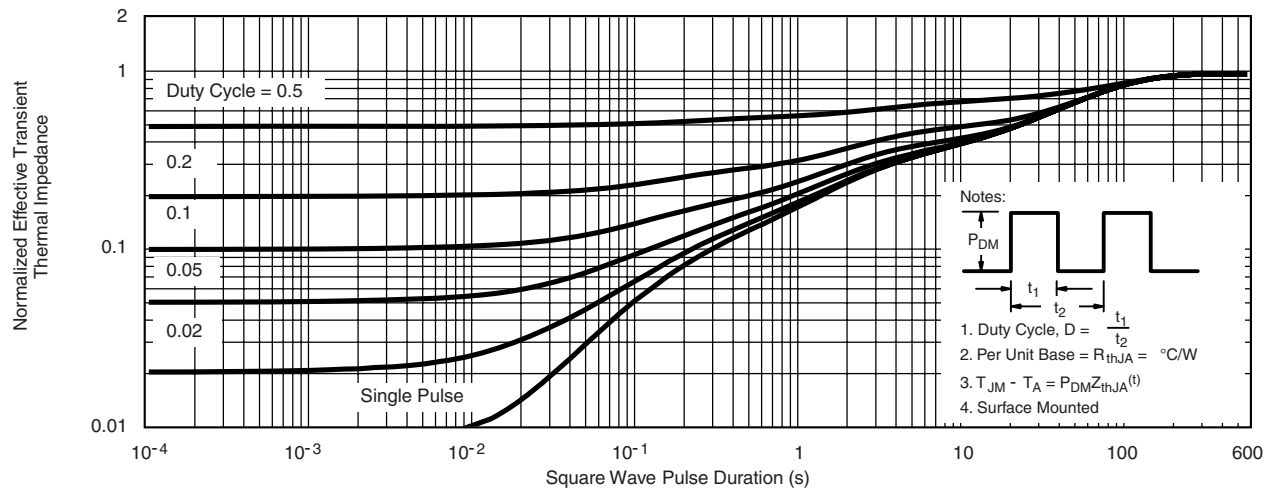


Safe Operating Area, Junction-to-Ambient

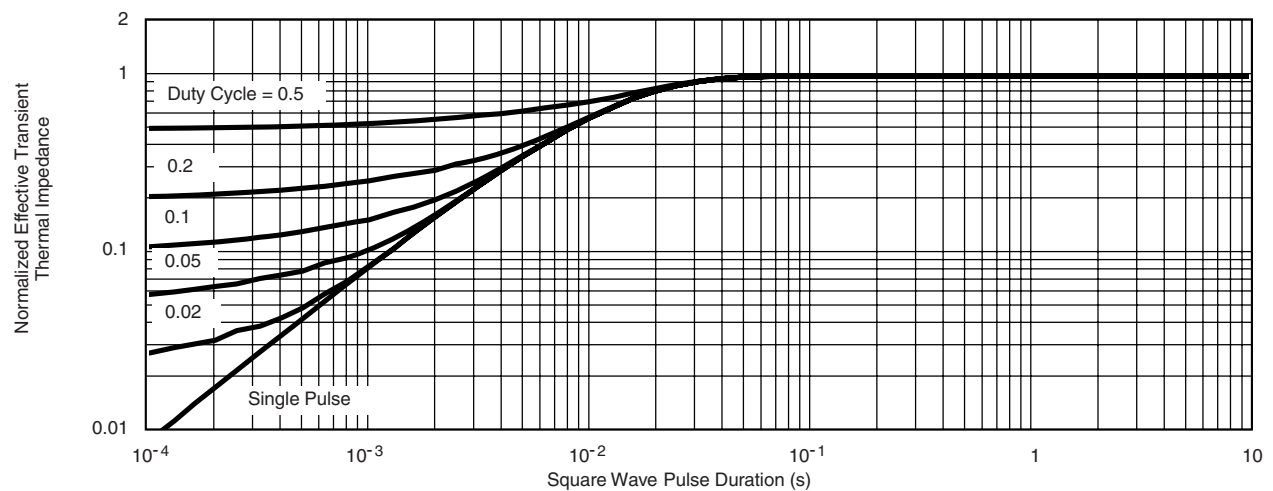
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Current Derating*****Single Pulse Avalanche Capability****Power, Junction-to-Case****Power, Junction-to-Ambient**

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



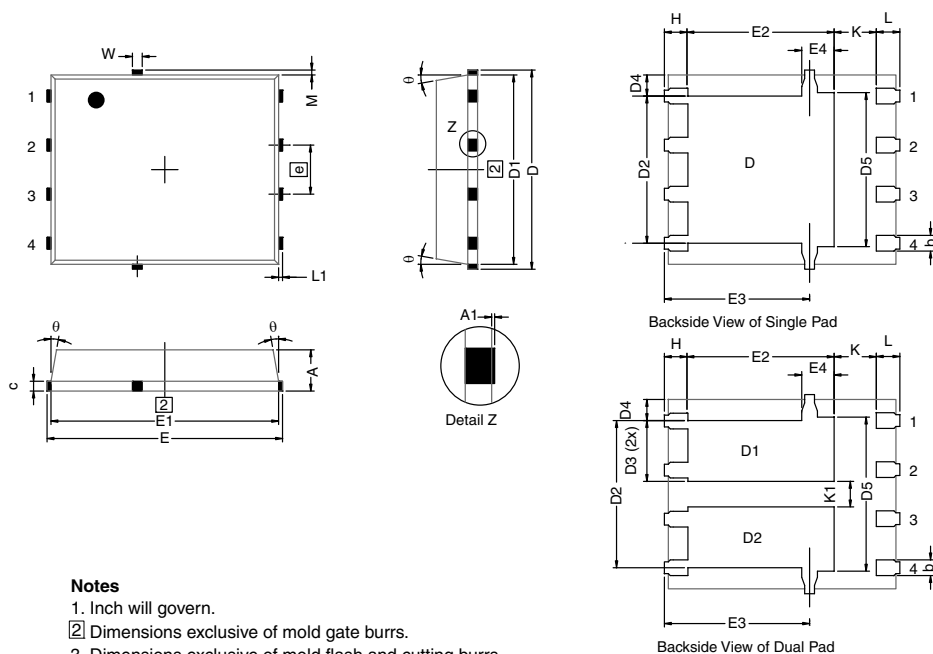
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

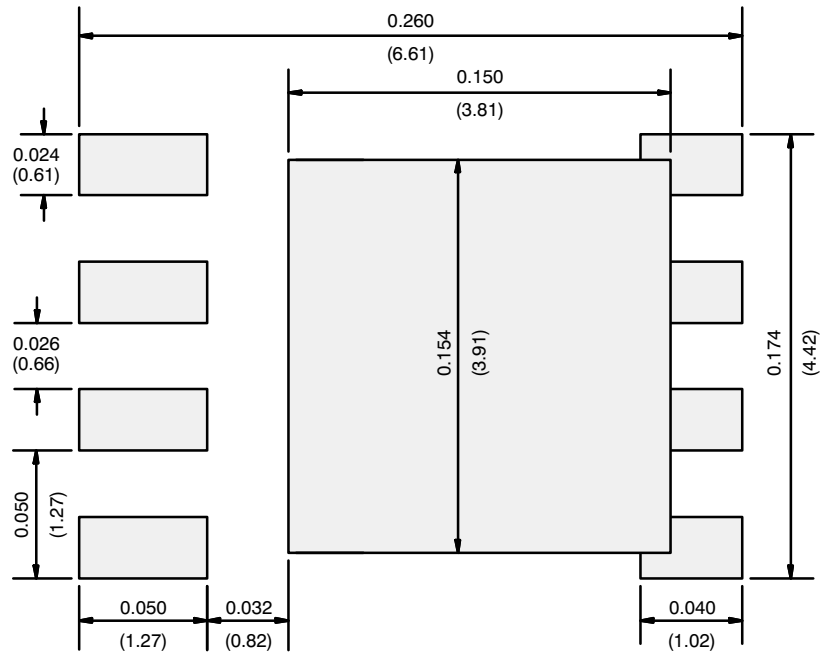
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PowerPAK® SO-8, (Single/Dual)



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1		-	0.05	0	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4	0.57 typ.			0.0225 typ.		
D5	3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2 (for AL product)	3.30	3.48	3.66	0.130	0.137	0.144
E2 (for other product)	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4 (for AL product)	0.58 typ.			0.023 typ.		
E4 (for other product)	0.75 typ.			0.030 typ.		
e	1.27 BSC			0.050 BSC		
K (for AL product)	1.45 typ.			0.057 typ.		
K (for other product)	1.27 typ.			0.050 typ.		
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: C13-0702-Rev. K, 20-May-13						
DWG: 5881						

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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