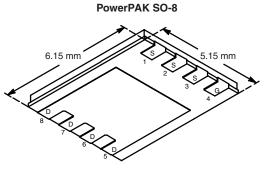


Vishay Siliconix

COMPLIANT

N-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	R_{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)		
12	0.0026 at V_{GS} = 4.5 V	29	54		
	0.0037 at V _{GS} = 2.5 V	23	54		



Bottom View

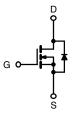
Ordering Information: Si7858ADP-T1-E3 (Lead (Pb)-free) Si7858ADP-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free available
- TrenchFET[®] Power MOSFET
- New Low Thermal Resistance PowerPAK[®] Package with Low 1.07 mm Profile
- 100 % R_g Tested

APPLICATIONS

 Low Output Voltage, High Current Synchronous Rectifiers



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_{μ}	$x = 25 \circ C$, unles	ss otherwise n	oted			
Parameter		Symbol	10 s	Steady State	Unit	
Drain-Source Voltage		V _{DS}	12		V	
Gate-Source Voltage		V _{GS}	± 8			
Continuous Drain Current (T _{.1} = 150 °C) ^a	T _A = 25 °C	– I _D	29	20	А	
Continuous Drain Current $(1_j = 150^{\circ} C)$	T _A = 70 °C		23	16		
Pulsed Drain Current (10 µs Pulse Width)		I _{DM}	60		A	
Continuous Source Current (Diode Conduction) ^a		۱ _S	4.5	1.6		
Maximum Dawar Dissinction	T _A = 25 °C	PD	5.4	1.9	W	
Maximum Power Dissipation ^a	T _A = 70 °C	۰D	3.4	1.2	vv	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		0°	
Soldering Recommendations (Peak Temperature) ^{b,c}			2	260	0	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Mariana lucation to Ambianta	t ≤ 10 s	R _{thJA}	18	23	
Maximum Junction-to-Ambient ^a	Steady State	' 'thJA	50	65	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	1.0	1.5	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static					•		
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	0.6	0.95	1.5	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 8$ V			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 12 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1		
Zero Gale voltage Drain Current		V_{DS} = 12 V, V_{GS} = 0 V, T_{J} = 55 °C			10	μA	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5$ V, $V_{GS} = 4.5$ V	30			А	
	Б	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 29 \text{ A}$		0.0020	0.0026	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 2.5 \text{ V}, \text{ I}_{D} = 23 \text{ A}$		0.0029	0.0037		
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 6 V, I_{D} = 29 A$		130		S	
Diode Forward Voltage ^a	V _{SD}	$I_{S} = 2.9 \text{ A}, V_{GS} = 0 \text{ V}$		0.75	1.1	V	
Dynamic ^b							
Input Capacitance	C _{iss}			5700			
Output Capacitance	C _{oss}	³⁵ ss V _{DS} = 6 V, V _{SS} = 0 V, f = 1 MHz		2680		pF	
Reverse Transfer Capacitance	C _{rss}			1280			
Total Gate Charge	Qg			54	80		
Gate-Source Charge	Q _{gs}	V_{DS} = 6 V, V_{GS} = 4.5 V, I_D = 29 A		10		nC	
Gate-Drain Charge	Q _{gd}			16		1	
Gate Resistance	Rg		0.5	1.2	2.0	Ω	
Turn-On Delay Time	t _{d(on)}			40	60		
Rise Time	t _r	$V_{DD} = 6 \text{ V}, \text{ R}_{L} = 6 \Omega$		40	60	ns	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω		140	210		
Fall Time	t _f			70	100]	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.9 A, di/dt = 100 A/μs		50	80		

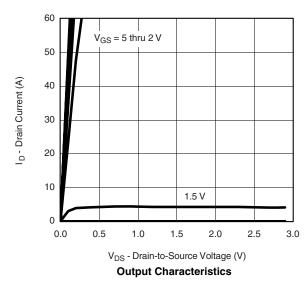
Notes:

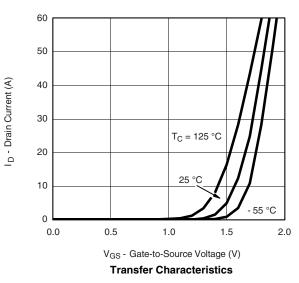
a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

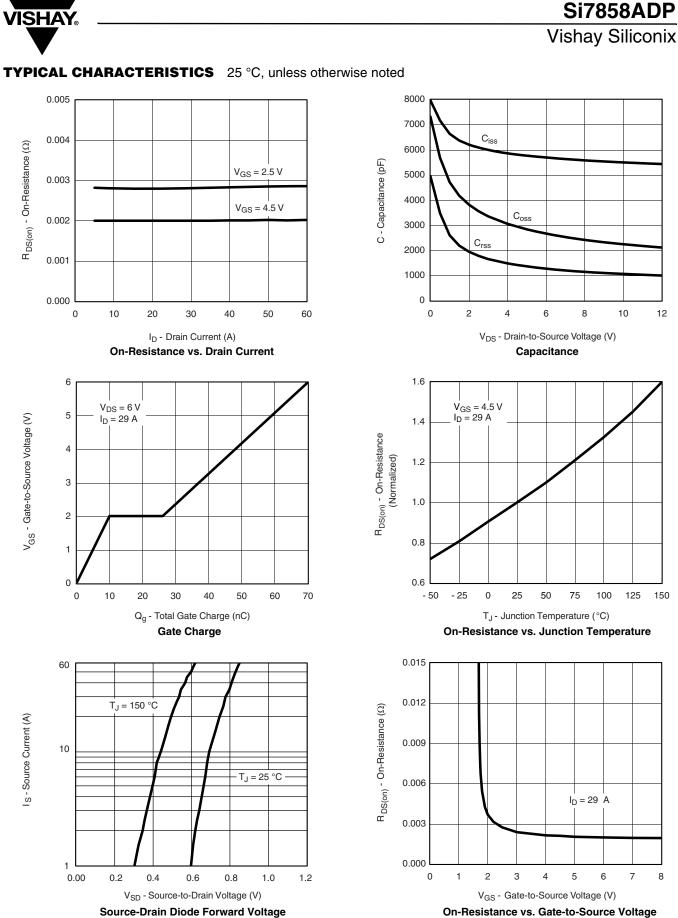
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted







Document Number: 73164 S-80440-Rev. C, 03-Mar-08

Si7858ADP

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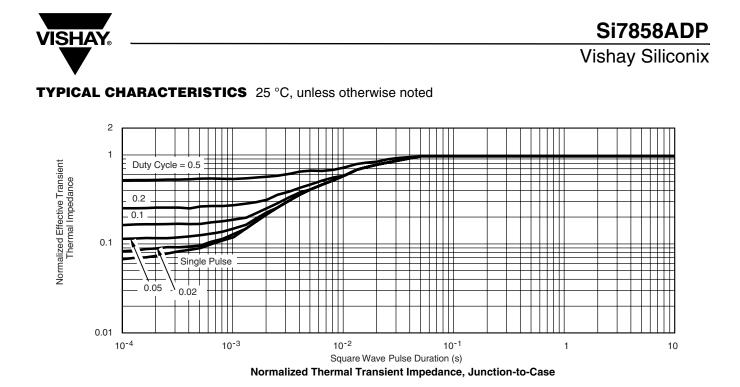
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

0.4 200 0.2 160 $I_D = 250 \ \mu A$ 0.0 V_{GS(th)} Variance (V) Power (W) 120 - 0.2 - 0.4 80 - 0.6 40 - 0.8 - 1.0 0 - 25 0 75 150 - 50 25 50 100 125 0.001 0.01 0.1 1 10 T_J - Temperature (°C) Time (s) **Threshold Voltage** Single Pulse Power 100 Limited by R_{DS(c} 1 ms 10 ms 10 I D - Drain Current (A) 100 ms 1 s 10 s DC 0.1 $T_C = 25 \ ^{\circ}C$ Single Pulse 0.01 0.01 0.1 10 100 1 V_{DS} - Drain-to-Source Voltage (V) * V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified Safe Operating Area Junction-to-Case 2 1 Normalized Effective Transient Thermal Impedance Duty Cycle = 0.5 1111 0.2 ТП Notes 0.1 P_{DM} 0.1 0.05 t₁ t2 t₁ 1. Duty Cycle, D = 0.02 1. Duty Cycle, D = $\frac{t_2}{t_2}$ 2. Per Unit Base = R_{thJA} = 50 °C//W 3. T_{JM} - $T_A = P_{DM}Z_{thJA}^{(t)}$ Single Pulse 4. Surface Mounted 0.01 10⁻³ 10⁻² 10-4 10-1 600 1 10 100 Square Wave Pulse Duration (s)

Normalized Thermal Transient Impedance, Junction-to-Ambient

4





Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?73164.



Vishay Siliconix

PowerPAK[®] SO-8, (Single/Dual)









Backside View of Dual Pad

Notes

1. Inch will govern.

2 Dimensions exclusive of mold gate burrs.

3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.97	1.04	1.12	0.038	0.041	0.044	
A1		-	0.05	0	-	0.002	
b	0.33	0.41	0.51	0.013	0.016	0.020	
С	0.23	0.28	0.33	0.009	0.011	0.013	
D	5.05	5.15	5.26	0.199	0.203	0.207	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.56	3.76	3.91	0.140	0.148	0.154	
D3	1.32	1.50	1.68	0.052	0.059	0.066	
D4	0.57 typ.				0.0225 typ.		
D5		3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246	
E1	5.79	5.89	5.99	0.228	0.232	0.236	
E2 (for AL product)	3.30	3.48	3.66	0.130	0.137	0.144	
E2 (for other product)	3.48	3.66	3.84	0.137	0.144	0.151	
E3	3.68	3.78	3.91	0.145	0.149	0.154	
E4 (for AL product)		0.58 typ.		0.023 typ.			
E4 (for other product)	0.75 typ.			0.030 typ.			
е	1.27 BSC			0.050 BSC			
K (for AL product)	1.45 typ.			0.057 typ.			
K (for other product)	1.27 typ.			0.050 typ.			
K1	0.56	-	-	0.022	-	-	
Н	0.51	0.61	0.71	0.020	0.024	0.028	
L	0.51	0.61	0.71	0.020	0.024	0.028	
L1	0.06	0.13	0.20	0.002	0.005	0.008	
θ	0°	-	12°	0°	-	12°	
W	0.15	0.25	0.36	0.006	0.010	0.014	
М	0.125 typ.			0.005 typ.			

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Application Note 826

Vishay Siliconix

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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Vishay

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