

Dual N-Channel 150-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
150	0.150 at $V_{GS} = 10$ V	3.3
	0.168 at $V_{GS} = 6$ V	3.1

FEATURES

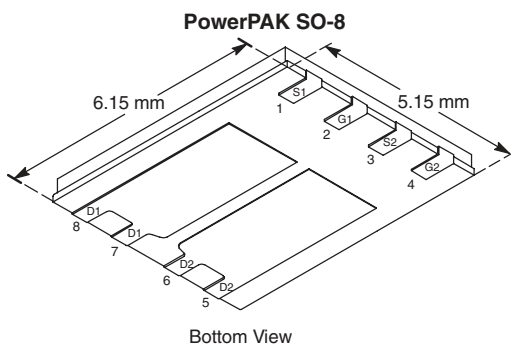
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFETs
- New Low Thermal Resistance PowerPAK® Package
- Dual MOSFET for Space Savings
- PWM Optimized for Fast Switching
- Avalanche Rated



RoHS
COMPLIANT
HALOGEN
FREE
Available

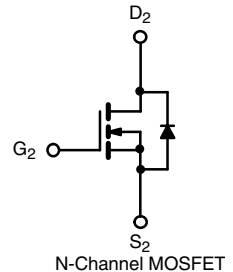
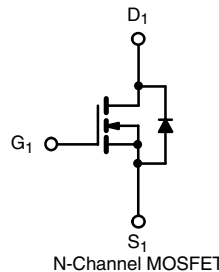
APPLICATIONS

- Primary Side Switch



Bottom View

Ordering Information: Si7946DP-T1-E3 (Lead (Pb)-free)
Si7946DP-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V _{DS}	150		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	3.3	2.1	A
	T _A = 70 °C		2.6	1.7	
Pulsed Drain Current		I _{DM}	10		
Continuous Source Current (Diode Conduction) ^a		I _S	2.9	1.2	
Single Avalanche Current	L = 0.1 mH	I _{AS}	9		
Single Avalanche Energy		E _{AS}	4		mJ
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	3.5	1.4	W
	T _A = 70 °C		2.2	0.9	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b, c}			260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	26	35	$^\circ\text{C/W}$
		60	85	
Maximum Junction-to-Case (Drain)	R_{thJC}	3.2	4.2	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

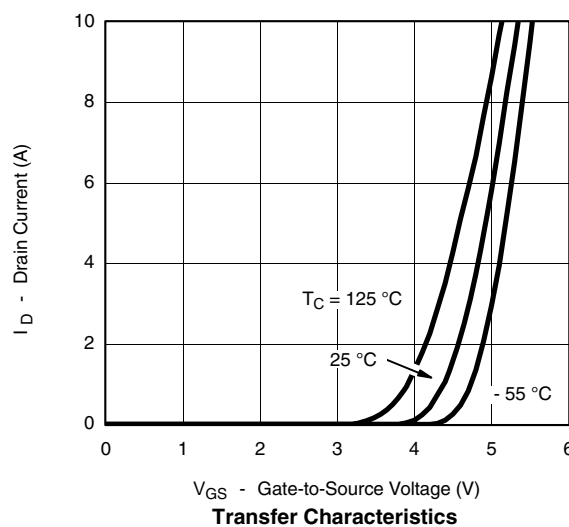
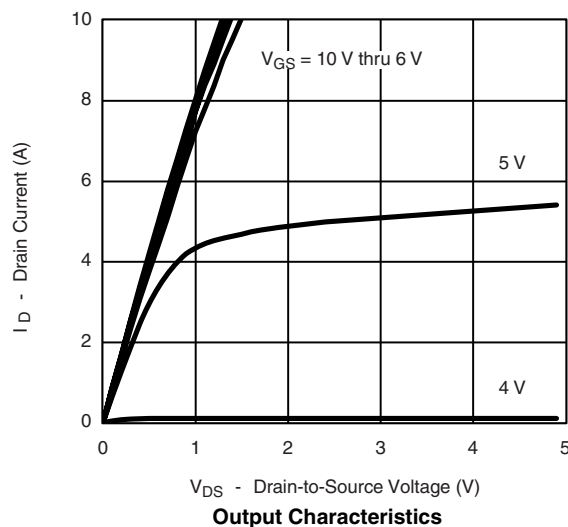
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2		4.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 150\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 150\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	10			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 3.3\ \text{A}$		0.124	0.150	Ω
		$V_{GS} = 6\ \text{V}$, $I_D = 3.1\ \text{A}$		0.137	0.168	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 3.3\ \text{A}$		9		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.9\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.87	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 75\ \text{V}$, $V_{GS} = 10\ \text{V}$, $I_D = 3.3\ \text{A}$		12.6	20	nC
Gate-Source Charge	Q_{gs}			2.8		
Gate-Drain Charge	Q_{gd}			4.5		
Gate Resistance	R_g	$f = 1\ \text{MHz}$		3.5		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 75\ \text{V}$, $R_L = 75\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_g = 6\ \Omega$		11	20	ns
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			30	45	
Fall Time	t_f			20	30	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.9\ \text{A}$, $dI/dt = 100\ \text{A}/\mu\text{s}$		62	100	

Notes:

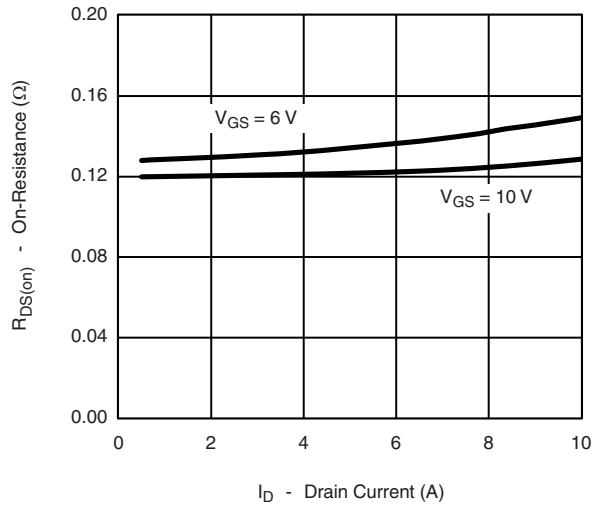
a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

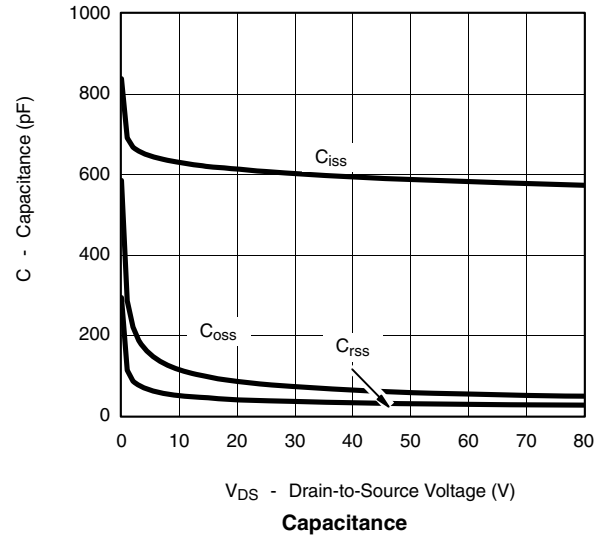
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25°C , unless otherwise noted

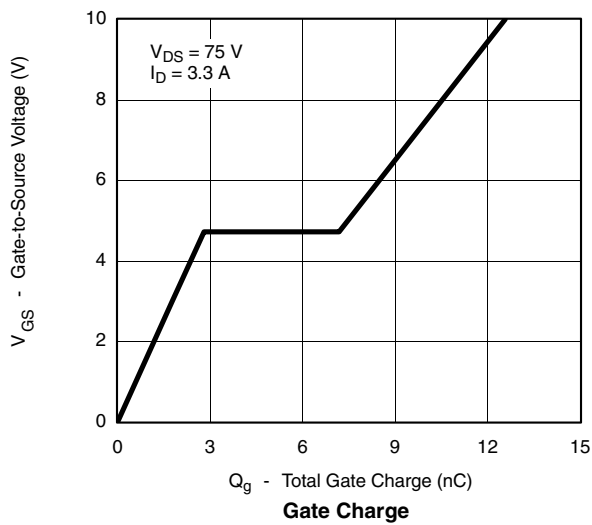
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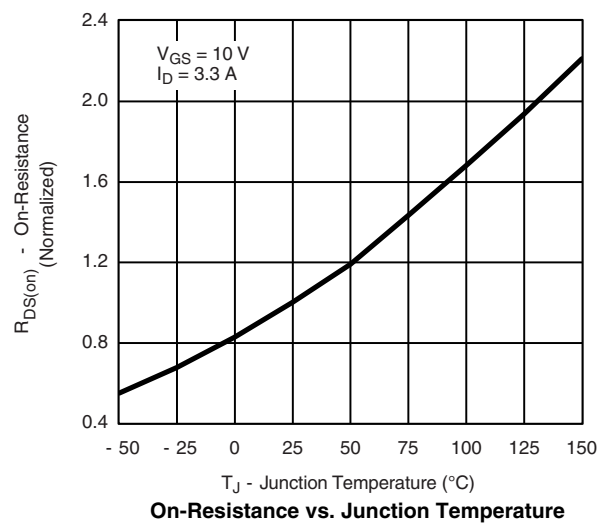
On-Resistance vs. Drain Current



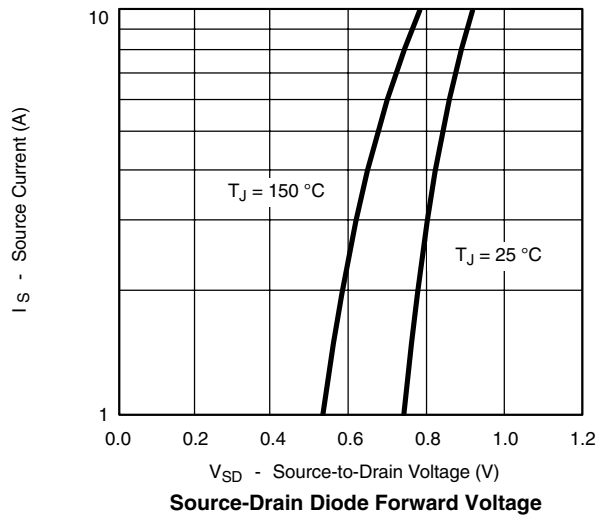
Capacitance



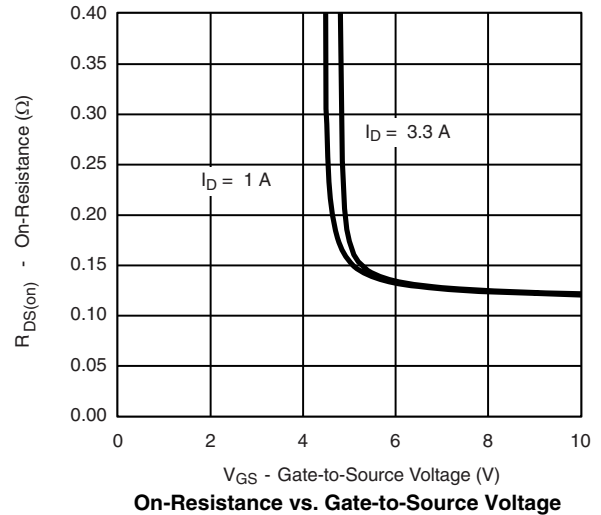
Gate Charge



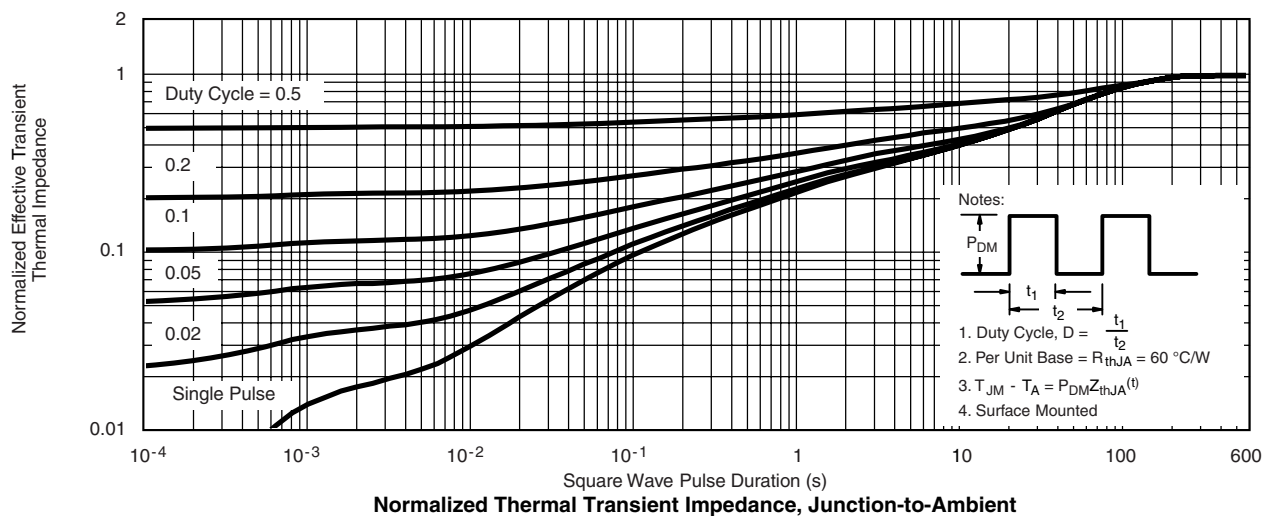
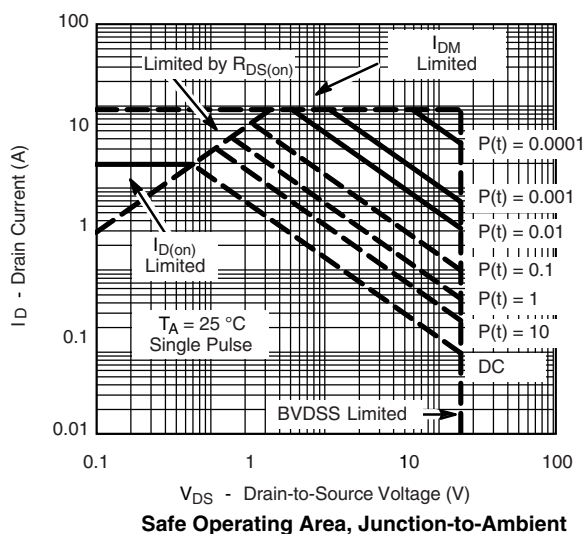
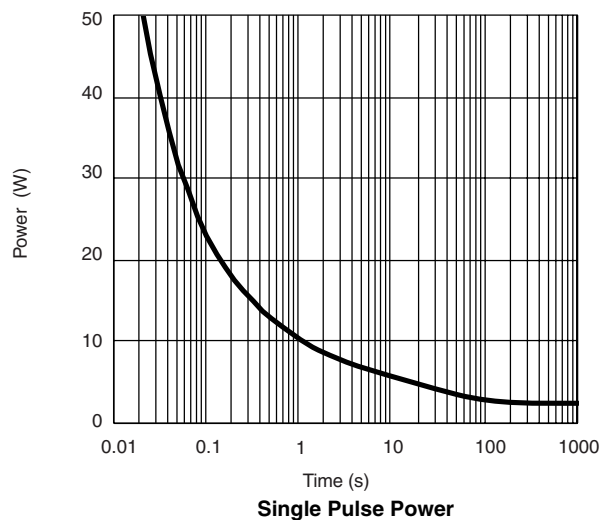
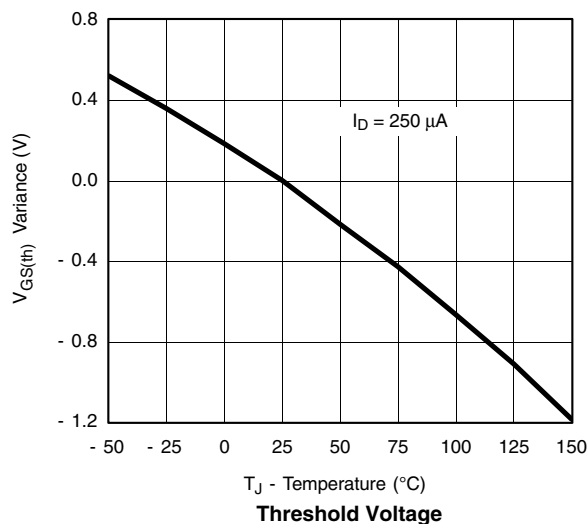
On-Resistance vs. Junction Temperature



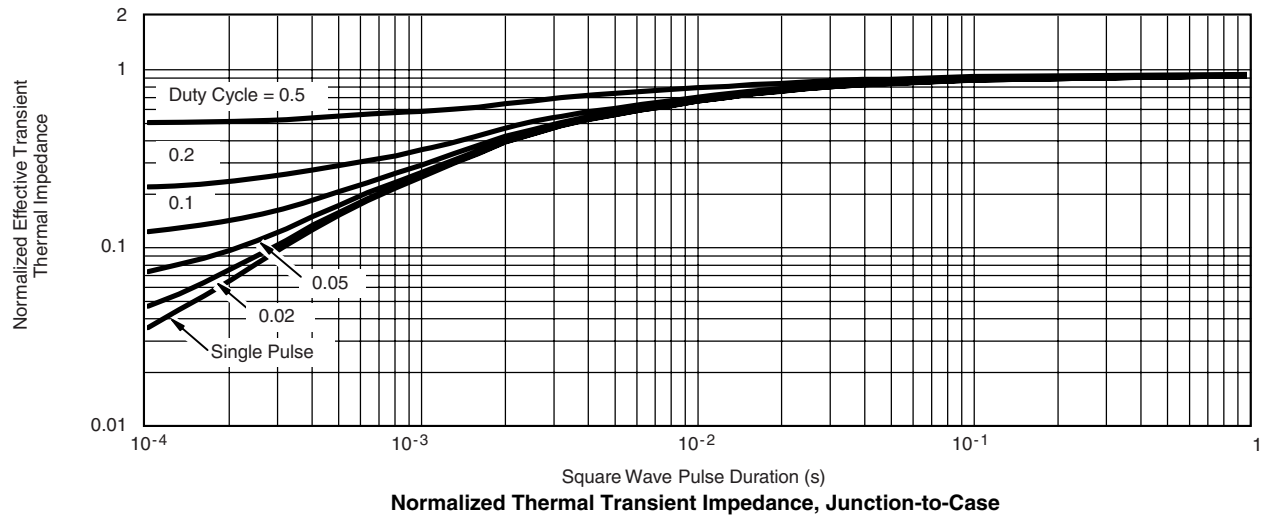
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

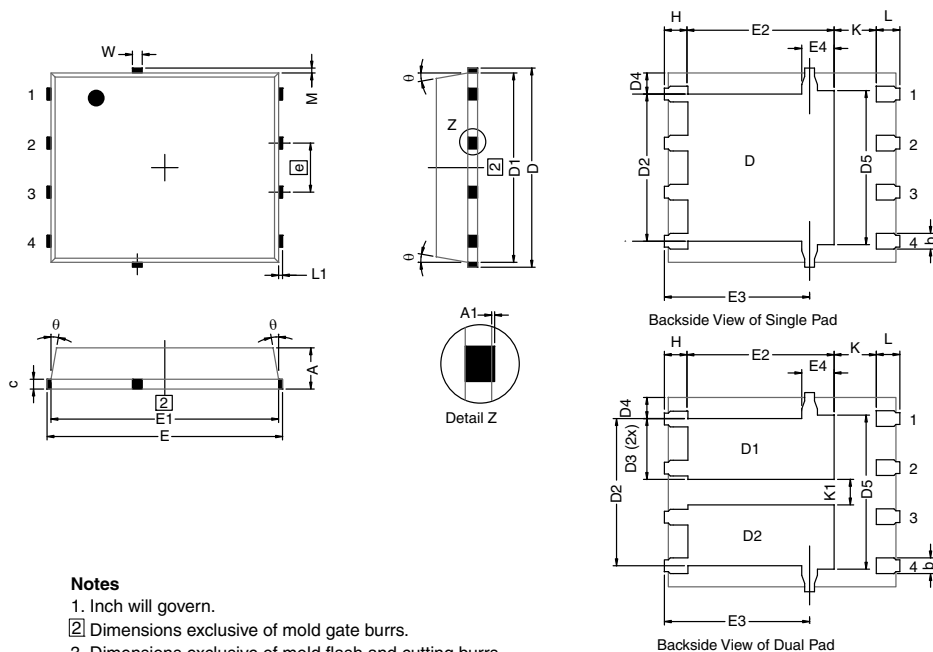
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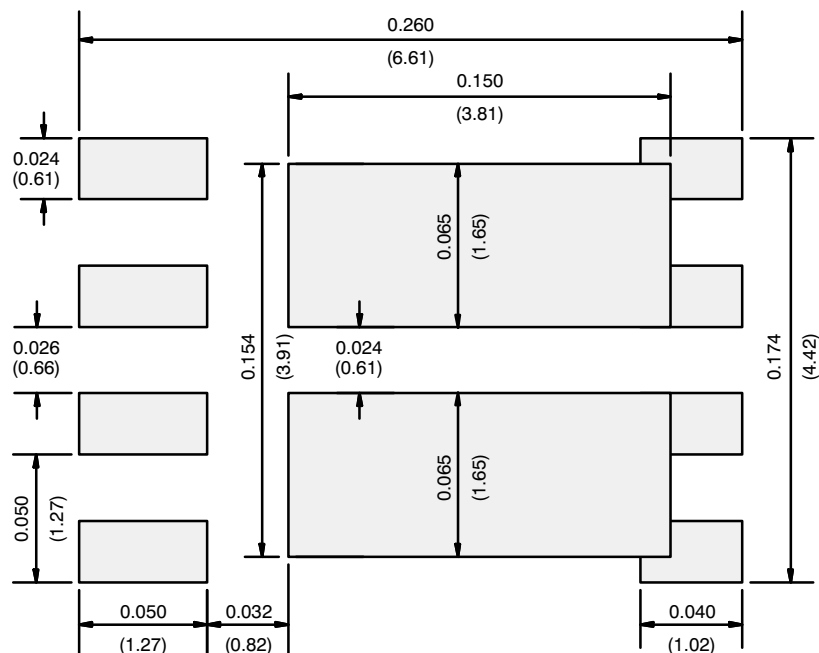
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PowerPAK® SO-8, (Single/Dual)



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1		-	0.05	0	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4	0.57 typ.			0.0225 typ.		
D5	3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2 (for AL product)	3.30	3.48	3.66	0.130	0.137	0.144
E2 (for other product)	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4 (for AL product)	0.58 typ.			0.023 typ.		
E4 (for other product)	0.75 typ.			0.030 typ.		
e	1.27 BSC			0.050 BSC		
K (for AL product)	1.45 typ.			0.057 typ.		
K (for other product)	1.27 typ.			0.050 typ.		
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: C13-0702-Rev. K, 20-May-13						
DWG: 5881						

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Dual



Recommended Minimum Pads Dimensions in Inches/(mm)

[Return to Index](#)



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