

# Power management (dual transistors)

## UMF6N

2SA2018 and 2SK3019 are housed independently in a UMT package.

### ●Application

Power management circuit

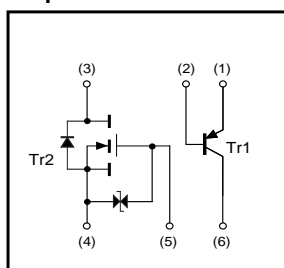
### ●Features

- 1) Power switching circuit in a single package.
- 2) Mounting cost and area can be cut in half.

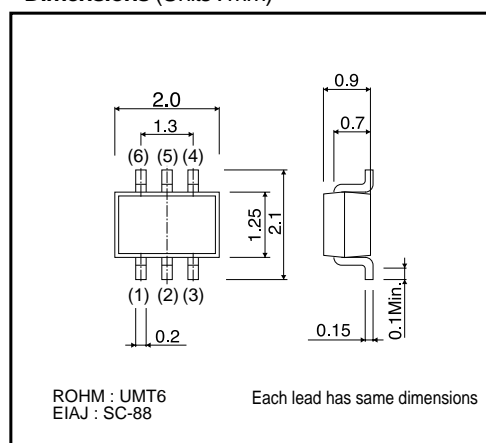
### ●Structure

Silicon epitaxial planar transistor

### ●Equivalent circuits



### ●Dimensions (Units : mm)



### ●Packaging specifications

|                              |       |
|------------------------------|-------|
| Type                         | UMF6N |
| Package                      | UMT6  |
| Marking                      | F6    |
| Code                         | TR    |
| Basic ordering unit (pieces) | 3000  |

## Transistors

## ●Absolute maximum ratings (Ta=25°C)

Tr1

| Parameter                    | Symbol           | Limits      | Unit  |
|------------------------------|------------------|-------------|-------|
| Collector-base voltage       | V <sub>CB0</sub> | -15         | V     |
| Collector-emitter voltage    | V <sub>CEO</sub> | -12         | V     |
| Emitter-base voltage         | V <sub>EBO</sub> | -6          | V     |
| Collector current            | I <sub>C</sub>   | -500        | mA    |
|                              | I <sub>CP</sub>  | -1.0        | A *1  |
| Power dissipation            | P <sub>C</sub>   | 150(TOTAL)  | mW *2 |
| Junction temperature         | T <sub>j</sub>   | 150         | °C    |
| Range of storage temperature | T <sub>stg</sub> | -55 to +150 | °C    |

\*1 Single pulse P<sub>W</sub>=1ms

\*2 120mW per element must not be exceeded. Each terminal mounted on a recommended land.

Tr2

| Parameter                    | Symbol           | Limits           | Unit      |
|------------------------------|------------------|------------------|-----------|
| Drain-source voltage         | V <sub>DSS</sub> | 30               | V         |
| Gate-source voltage          | V <sub>GSS</sub> | ±20              | V         |
| Drain current                | Continuous       | I <sub>D</sub>   | 100 mA    |
|                              | Pulsed           | I <sub>DP</sub>  | 200 mA *1 |
| Reverse drain current        | Continuous       | I <sub>DR</sub>  | 100 mA    |
|                              | Pulsed           | I <sub>DRP</sub> | 200 mA *1 |
| Total power dissipation      | P <sub>D</sub>   | 150(TOTAL)       | mW *2     |
| Channel temperature          | T <sub>ch</sub>  | 150              | °C        |
| Range of storage temperature | T <sub>stg</sub> | -55 to +150      | °C        |

\*1 P<sub>W</sub>≤10ms Duty cycle≤50%

\*2 120mW per element must not be exceeded. Each terminal mounted on a recommended land.

## ●Electrical characteristics (Ta=25°C)

Tr1

| Parameter                            | Symbol               | Min. | Typ. | Max. | Unit | Conditions   |
|--------------------------------------|----------------------|------|------|------|------|--|
| Collector-emitter breakdown voltage  | BV <sub>CEO</sub>    | -12  | -    | -    | V    | I <sub>C</sub> =-1mA                                 |
| Collector-base breakdown voltage     | BV <sub>CB0</sub>    | -15  | -    | -    | V    | I <sub>C</sub> =-10μA                                |
| Emitter-base breakdown voltage       | BV <sub>EBO</sub>    | -6   | -    | -    | V    | I <sub>E</sub> =-10μA                                |
| Collector cut-off current            | I <sub>CB0</sub>     | -    | -    | -100 | nA   | V <sub>CB</sub> =-15V                                |
| Emitter cut-off current              | I <sub>EBO</sub>     | -    | -    | -100 | nA   | V <sub>EB</sub> =-6V                                 |
| Collector-emitter saturation voltage | V <sub>CE(sat)</sub> | -    | -100 | -250 | mV   | I <sub>C</sub> =-200mA, I <sub>B</sub> =-10mA        |
| DC current gain                      | h <sub>FE</sub>      | 270  | -    | 680  | -    | V <sub>CE</sub> =-2V, I <sub>C</sub> =-10mA          |
| Transition frequency                 | f <sub>T</sub>       | -    | 260  | -    | MHz  | V <sub>CE</sub> =-2V, I <sub>E</sub> =10mA, f=100MHz |
| Collector output capacitance         | C <sub>ob</sub>      | -    | 6.5  | -    | pF   | V <sub>CB</sub> =-10V, I <sub>E</sub> =0mA, f=1MHz   |

Tr2

| Parameter                               | Symbol               | Min. | Typ. | Max. | Unit | Conditions   |
|---|----------------------|------|------|------|------|--|
| Gate-source leakage                     | I <sub>GSS</sub>     | -    | -    | ±1   | μA   | V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V   |
| Drain-source breakdown voltage          | V <sub>(BR)DSS</sub> | 30   | -    | -    | V    | I <sub>D</sub> =10μA, V <sub>GS</sub> =0V  |
| Zero gate voltage drain current         | I <sub>DSS</sub>     | -    | -    | 1.0  | μA   | V <sub>DS</sub> =30V, V <sub>GS</sub> =0V  |
| Gate-threshold voltage                  | V <sub>GS(th)</sub>  | 0.8  | -    | 1.5  | V    | V <sub>DS</sub> =3V, I <sub>D</sub> =100μA   |
| Static drain-source on-state resistance | R <sub>DS(on)</sub>  | -    | 5    | 8    | Ω    | I <sub>D</sub> =10mA, V <sub>GS</sub> =4V  |
|   |                      | -    | 7    | 13   | Ω    | I <sub>D</sub> =1mA, V <sub>GS</sub> =2.5V   |
| Forward transfer admittance             | Y <sub>fs</sub>      | 20   | -    | -    | ms   | V <sub>DS</sub> =3V, I <sub>D</sub> =10mA  |
| Input capacitance                       | C <sub>iss</sub>     | -    | 13   | -    | pF   | V <sub>DS</sub> =5V, V <sub>GS</sub> =0V, f=1MHz   |
| Output capacitance                      | C <sub>oss</sub>     | -    | 9    | -    | pF   |  |
| Reverse transfer capacitance            | C <sub>rss</sub>     | -    | 4    | -    | pF   |  |
| Turn-on delay time                      | t <sub>d(on)</sub>   | -    | 15   | -    | ns   |  |
| Rise time                               | t <sub>r</sub>       | -    | 35   | -    | ns   | I <sub>D</sub> =10mA, V <sub>DD</sub> =5V,<br>V <sub>GS</sub> =5V, R <sub>L</sub> =500Ω,<br>R <sub>GS</sub> =10Ω |
| Turn-off delay time                     | t <sub>d(off)</sub>  | -    | 80   | -    | ns   |  |
| Fall time                               | t <sub>f</sub>       | -    | 80   | -    | ns   |  |

Transistors

●Electrical characteristic curves

Tr1

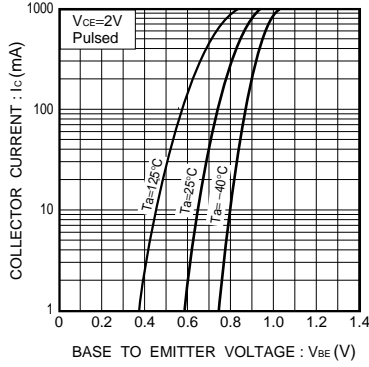


Fig.1 Grounded emitter propagation characteristics

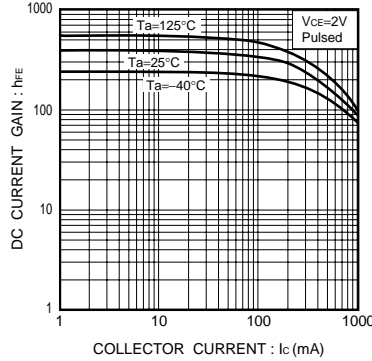


Fig.2 DC current gain vs. collector current

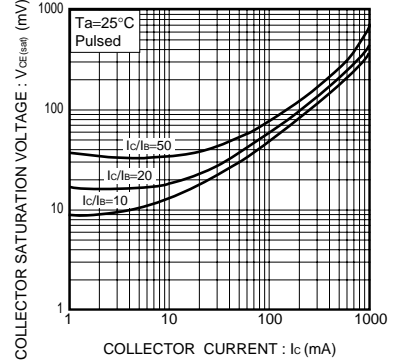


Fig.3 Collector-emitter saturation voltage vs. collector current ( I )

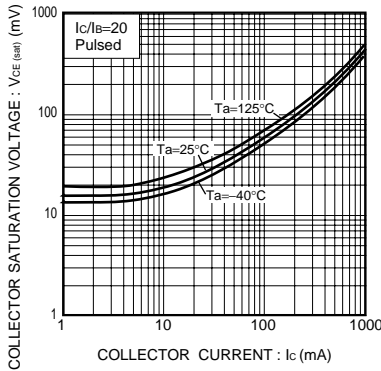


Fig.4 Collector-emitter saturation voltage vs. collector current ( II )

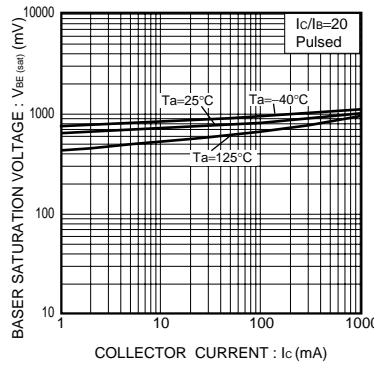


Fig.5 Base-emitter saturation voltage vs. collector current

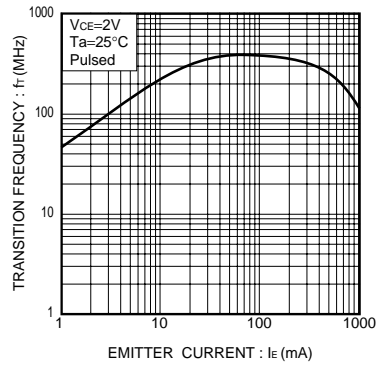


Fig.6 Gain bandwidth product vs. emitter current

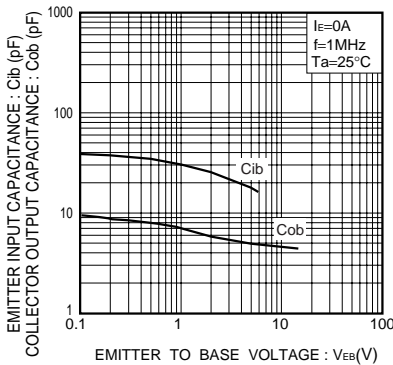


Fig.7 Collector output capacitance vs. collector-base voltage  
Emitter input capacitance vs. emitter-base voltage

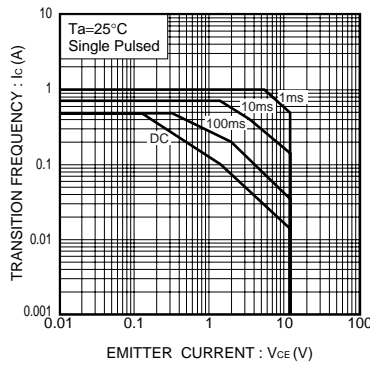


Fig.8 Safe operation area

Transistors

Tr2

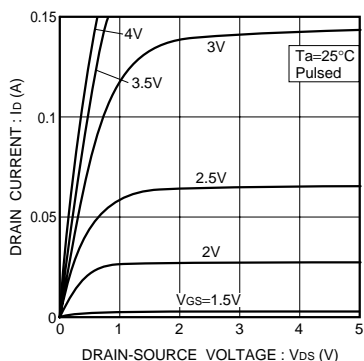


Fig.9 Typical output characteristics

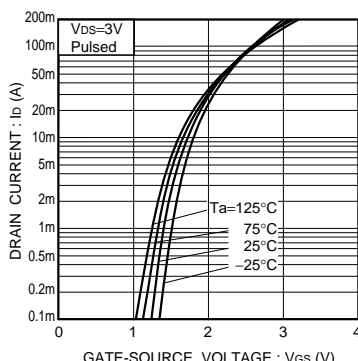


Fig.10 Typical transfer characteristics

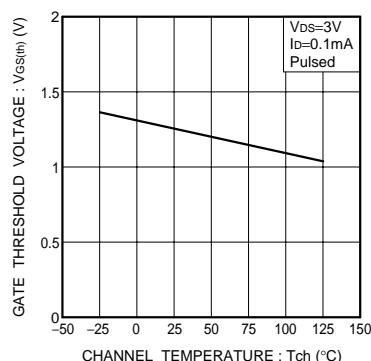


Fig.11 Gate threshold voltage vs. channel temperature

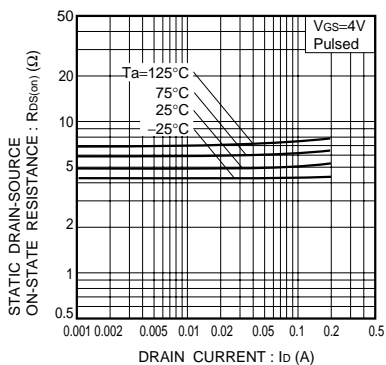


Fig.12 Static drain-source on-state resistance vs. drain current ( I )

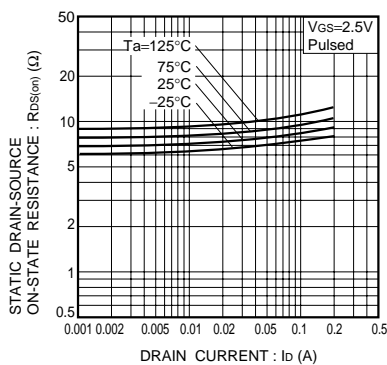


Fig.13 Static drain-source on-state resistance vs. drain current ( II )

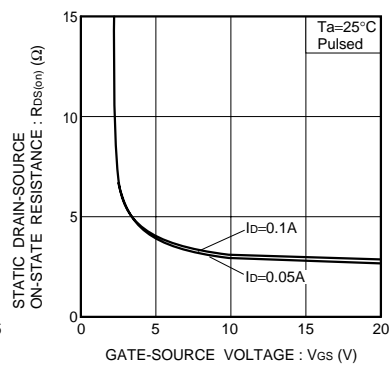


Fig.14 Static drain-source on-state resistance vs. gate-source voltage

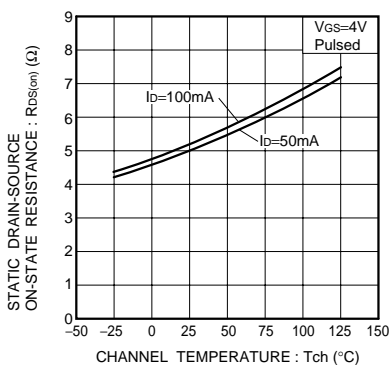


Fig.15 Static drain-source on-state resistance vs. channel temperature

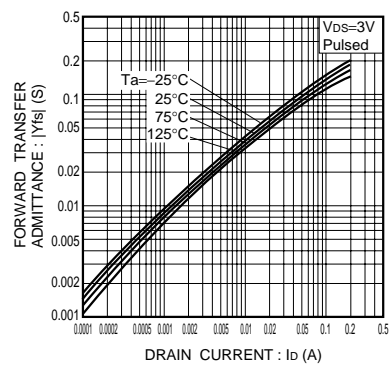


Fig.16 Forward transfer admittance vs. drain current

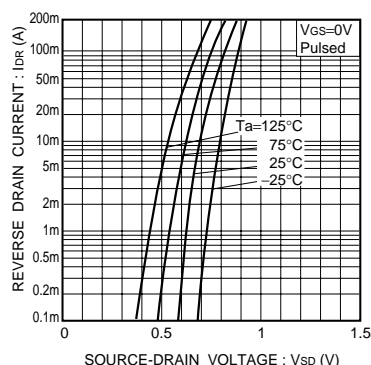


Fig.17 Reverse drain current vs. source-drain voltage ( I )

Transistors

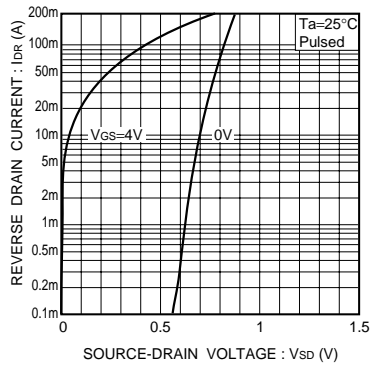


Fig.18 Reverse drain current vs. source-drain voltage ( II )

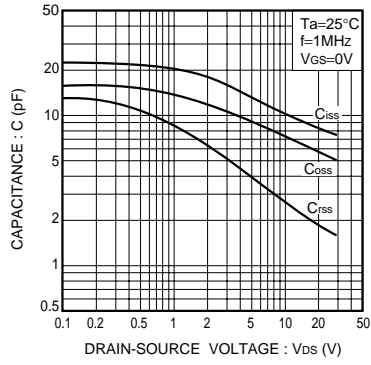


Fig.19 Typical capacitance vs. drain-source voltage

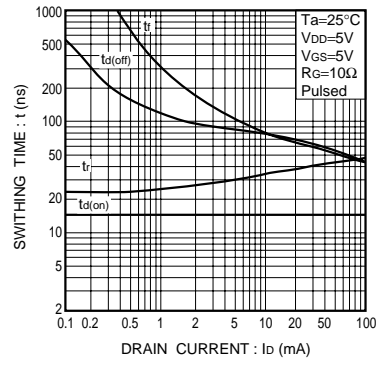


Fig.20 Switching characteristics

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