QF3DFX

Audio Filtering and Effects Processor

APPLICATIONS

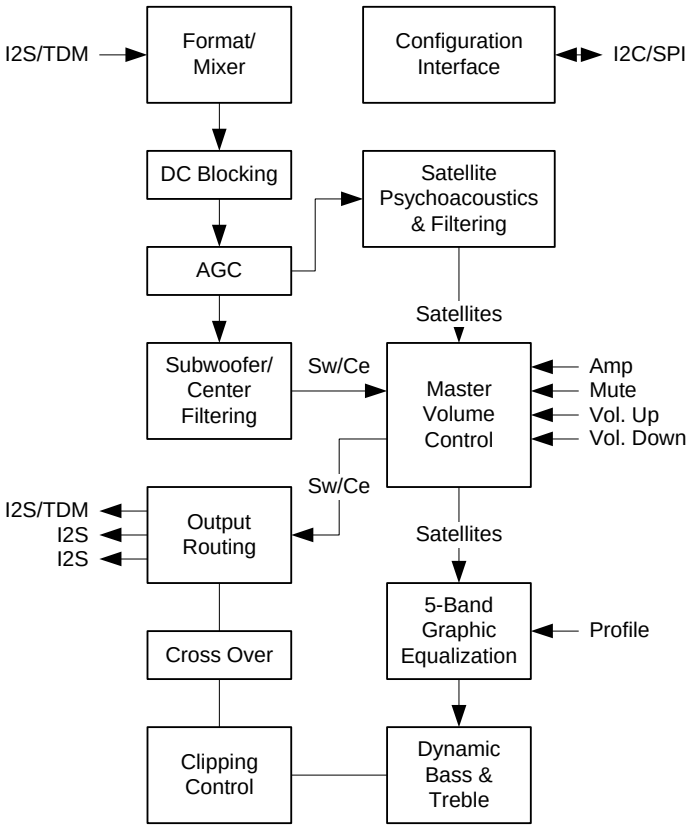
- **Powered Speaker Products**
- **Sound Bars**
- **Docking Stations**
- **Internet Radio**
- **MP3 Players**
- **Stereo Headsets (wired or wireless)**
- **Televisions**
- **Home Theatre**
- **Other audio products**

DESCRIPTION

A powerful 3-channel audio filter and effects system-on-a-chip designed for seamless insertion in an audio serial digital data path. The QF3DFX is easily configured using the Quickfilter's QFPro™ Design Software (QFPro) with royalty free user tunable advanced audio algorithms for psychoacoustic effects. The QF3DFX can be configured to interface with I2S or TDM based audio systems. The QF3DFX can operate over a broad range of data rates up to 48ksps and can support data resolutions of 16 or 24 bits. The QF3DFX is self-booting and provides pin control for volume up, volume down, mute and profiles supporting cost sensitive designs with minimal external requirements. The QF3DFX automatically powers down when audio data is not present.

KEY FEATURES

- **Input**
  - **I2S, 2-channels**
  - **TDM, up to 8-channels**
- **Output**
  - **2.2.1 (2.1 + crossover) or any subset**
  - **I2S x 3; 6-channels**
  - **TDM x 1; up to 8-channel frame**
- **DC Blocking**
- **AGC supports special modes**
  - **Night, Commercial, Dynamic Loudness**
- **Psychoacoustics**
  - **High Frequency Restoration**
  - **Spatialization**
  - **Virtual Bass**
- **Dynamic Bass and Treble**
- **Parametric Equalization**
- **User Controlled Graphic Equalization**
- **Profiles: Single-pin control with tone feedback**
- **Digital volume control with Mute**
- **Compression: Soft Clipper**
- **Advanced noise-shaping Bi-quad structure**
- **Self-booting**
- **Optional microcontroller can dynamically reconfigure system via I2C or SPI**
- **Low power: 1.8V Core, 1.8V – 3.3V IO, ~22 mW @ 48ksps, ~50 uW standby**
- **Cost effective**
  - **Microcontroller-less system; QF3DFX + EEPROM + 4 switches**



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2 PINOUT AND PIN DESCRIPTIONS

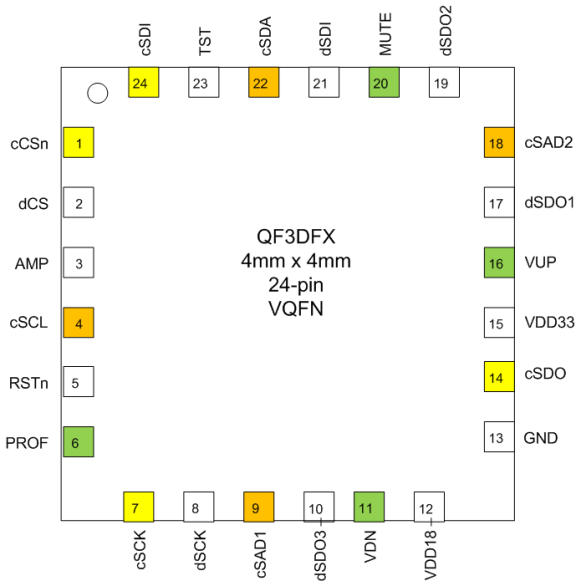


Figure 2-1 - 24 Pin QFN Package Pinout

Pin	Signal Name	I/O	Type	Description
1	cCSn	I	Digital	SPI configuration chip select; active low; default internal pull-up
2	dCS	I	Digital	I2S / TDM chip select; configurable as active low or high
3	AMP	I	Digital	Will Reduce overall amp gain by programmed value if asserted
4	cSCL	I/O	Digital	I2C configuration Clock
5	RSTn	I	Digital	Chip reset; active low; default internal pull-up
6	PROF	I	Digital	Round robin cycles through profiles
7	cSCK	I	Digital	SPI configuration input clock; rising capture edge
8	dSCK	I	Digital	I2S / TDM data input clock; either rising or falling capture edge
9	cSAD1	I	Digital	I2C configuration address 1
10	dSDO3	O	Digital	I2S data output
11	VDN	I	Digital	Volume Down
12	VDD18	N/A	Power	Digital Core voltage; 1.8V Fixed
13	GND	N/A	Return	Digital power supply return pin
14	cSDO	O	Digital	SPI configuration serial data output
15	VDD33	N/A	Power	Digital I/O voltage; 1.8V – 3.3V
16	VUP	I	Digital	Volume Up
17	dSDO1	O	Digital	I2S / TDM data output
18	cSAD2	I	Digital	I2C configuration address 2
19	dSDO2	O	Digital	I2S data output
20	MUTE	I	Digital	Mute
21	dSDI	I	Digital	I2S / TDM serial data input
22	cSDA	I/O	Digital	I2C configuration Data
23	TST	I	Digital	Test Mode – Tie to GND or let float
24	cSDI	I	Digital	SPI configuration data input

Table 2-1 Pin Descriptions

3 CLOCKING AND RESET

3.1 Clocking

There are minimal clocking requirements for the QF3DFX. The internal design is fully static; there is no internal dynamic circuitry. None of the clocks need to be continuously running.

cSCK and cSCL have no particular requirements aside from standard minimum high and low and max frequency limitations, usually due to their respective protocols. Both clocks can operate down to DC. Additional details can be found in the Timing Requirements section.

dSCK and dCS work together, and are typically generated from a crystal or other stable timebase. This is usually a requirement of the ADC's and DAC's they connect to. They do not need to be free running or continuously operating for the QF3DFX to operate. It is perfectly acceptable to freeze dSCK and dCS for power savings reasons, for example, and once they begin operating again, the QF3DFX will pick up exactly where it left off in the signal processing flow. Care should be taken that no clock glitches occur that may cause spurious data to enter the chip.

3.2 Power Ramping and Reset

The QF3DFX contains state logic that must be correctly initialized upon power-up before being used. This initialization is accomplished by having RSTn be asserted after V_{DD33} and V_{DD18} have reached valid operating levels as shown below. RSTn does not have to be high prior to being asserted. The low level alone will perform the initialization. There is no restriction on the relationship of the VDD33 ramp to the VDD18 ramp. Either may be ramped before the other or they may ramp together. However, both VDD33 and VDD18 must be at valid levels for the RSTn assertion to be recognized.

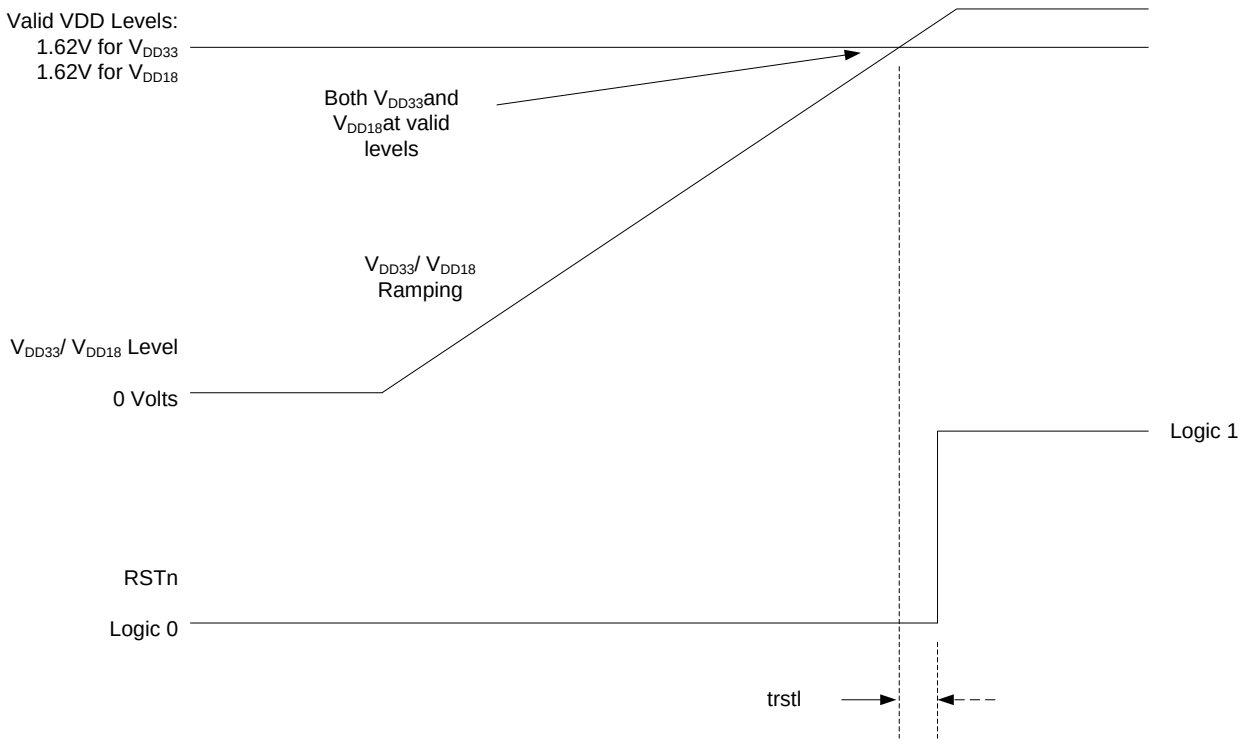


Figure 3-1 - Power-up Sequence and Reset

4 GENERAL DESCRIPTION

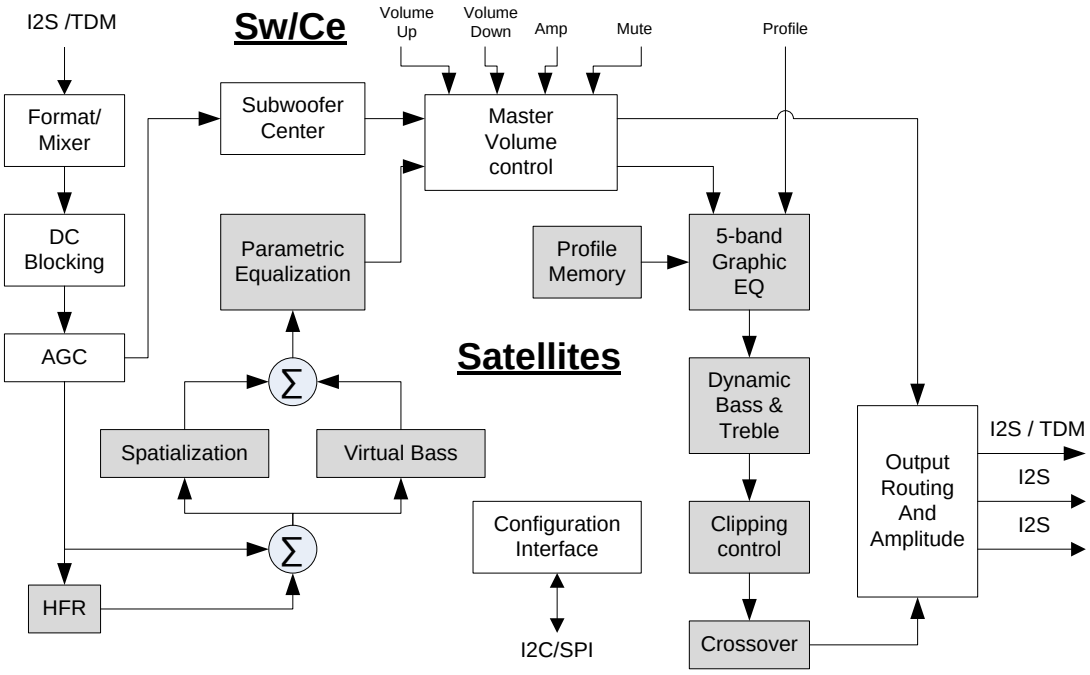


Figure 4-1 - Functional Block Diagram

4.1 General

The QF3DFX is internally a three channel audio filtering and effects system. The serial data interface can accept as input either 2 channels of I2S or up to 8 channels of TDM. The 3 internal audio channels are created by scaling and summing these incoming channels. All 3 channels receive DC blocking and automatic gain control. The Subwoofer/Center, Sw/Ce, channel is directed to a series of filters for band limiting and parametric equalization. The two satellite channels pass through psychoacoustic effects blocks consisting of high frequency restoration, virtual bass and spatialization. The satellite channels then pass through parametric equalization and enter a master volume block. The volume can be controlled externally via 3 pins; there is also provision for external amplifier thermal feedback compensation. The graphical equalization can also be externally controlled with one pin, profiles, with a provision for tone acknowledgement of the selected profile. Both the volume and graphical equalization can take on more elaborate forms of presentation in systems utilizing a microcontroller. Dynamic bass and treble are available for the satellite channels. Numerous forms of soft signal management are available to control clipping. The satellite channels have a crossover option creating 2 additional channels. The output is capable of routing any internal channel to any output port or slot position. Each output can have a unique gain value applied and, optionally, inverted.

Several QF3DFX devices can be used in series to process all the channels of a TDM stream or in parallel utilizing I2S.

4.2 Format/Mixer

Serial audio streams of 16 or 24-bit data of I2S, Left Justified, Right Justified, or TDM are supported. The input block creates 3-channels of audio data from these sources. For I2S data, the 2 satellite channels can be summed and reduced, user programmable, to form the 3rd channel. For TDM data, any of the channels within the TDM stream can be scaled and mixed to any of the 3 internal channels (2 satellite channels and 1 subwoofer/center channel).

The serial audio data can be in 2's complement or offset binary format with MSB first.

The QF3DFX utilizes the incoming bit clock and framing signal to exit power down mode and process the incoming serial audio data stream. The QF3DFX returns to power down mode when these are not active.

If desired, the QF3DFX can be bypassed. The bypass function simply routes the input (dSDI) to the output (dSDO1).

4.3 DC Blocking, DCB

This block provides the classic audio DC blocking filtering and is used to meet the overall system DC blocking rejection requirements.

4.4 Automatic Gain Control, AGC

The function of the of the AGC is to keep the input signal energy between the high and low threshold values, each with programmable gain, attack time and release time. The satellite channels share common configuration settings and the Sw/Ce channel has independent settings.

The attack time parameter controls how fast the signal is lowered when it is above high threshold while the release time parameter controls how fast the signal is raised when below the low threshold. The AGC can be programmed to ignore energy levels that are below the noise threshold value. The AGC is fully capable of supporting dynamic range compression.

The averaging time is programmable to support special modes such as Night mode and Commercial mode. Night mode prevents loud audio content when listening to audio at low levels. The AGC works to quickly reduce loud sounds only and does not increase quiet sounds. Commercial content has a higher energy value than the program content and is perceived as having more volume. The AGC works to quickly lower the commercial volume only without effecting program volume.

4.5 Subwoofer/Center, Sw/Ce

The Sw/Ce block provides an equalizing function for Sw/Ce channel processing. It is comprised of 7 biquad IIR filters for band limiting and parametric equalization. The Sw/Ce block output gain is independently adjustable for balancing with the satellite channel gain.

QFPro's parametric equalization design tool can be used to dynamically view composite results while selecting filter types (including custom; imported) and adjusting corresponding parameters.

4.6 High Frequency Restoration, HFR

The HFR block uses psychoacoustic techniques to help restore high frequency content that may have been lost due to audio compression or other processing. Many audio compression algorithms, such as that used with MP3 encoding, limit the high frequency content in order to reduce file size and transmission overhead. For reduced bit rate compressed audio, frequencies as low as 10 kHz may be removed. The HFR block restores this lost data. The HFR block can also be used on full-band audio to emphasize high frequency content, to compensate for speaker performance, as a system designer preference or to satisfy market requirements.

Using QFPro, this function is programmable and includes gain control for mixing the resulting effect back with the primary audio data. A common setting is applied to both satellite channels.

4.7 Spatialization, SP

The SP block uses a psychoacoustic algorithm to enhance the sense of stereo separation in an audio signal. Many audio platforms have speakers that are in close proximity, and therefore do not have the desired stereo separation or a sense of spaciousness. The SP block enhances the stereo separation that is present in audio data to increase the apparent speaker separation.

In conjunction with QFPro, the Spatialization function is highly configurable with fully independent main and effect processing for enhanced audio separation.

4.8 Virtual Bass, VB

With smaller enclosures come corresponding smaller speakers which often do not reproduce bass frequencies well. By using Quickfilter's VB psychoacoustic effects block, more apparent bass can be added to the satellite channels.

Common settings are utilized for both satellite channels. Using QFPro, this function is highly programmable and includes gain control for mixing the resulting effect back with the primary audio data.

4.9 Parametric Equalization, PEQ

The Parametric Equalizer is used to correct or adjust system and speaker related performance attributes and is comprised of ten 2nd-order IIR (biquad) filters in series. A common set of filter coefficients is applied to both satellite channels.

QFPro's parametric equalization design tool can be used to dynamically view composite results while selecting filter types (including custom; imported) and adjusting corresponding parameters.

4.10 Master Volume Control, MVC

The MVC comprises volume, mute, and amplifier protection features for both the satellite and Sw/Ce channels.

A single master gain value gets applied to each of the three channels. This gain can be varied from +24 to –102 dB (plus mute) in 1 dB steps. A user can sequence nonlinearly through this range two ways:

- A 100-step user-programmable table of volume levels. An index pointer can sequence up and down through this table under the control of the VUP and VDN pins, permitting the volume to increase and decrease in steps defined by the developer.
- Directly by a SPI or SIB bus master.

The MVC block also includes a user programmable slew rate to manage user-controlled volume changes.

Volume Up, Volume Down, and Mute can be controlled via the VUP, VDN, and MUTE pins, if desired. This method of controlling volume is useful if there is no external microcontroller in the system. At Power-on Reset, each pin is configured with an internal pull-up resistor enabled. Therefore, the only external hardware required to implement these functions is a momentary switch that, when closed, will drive the pin level to ground. Internal logic provides a debounce function; there is no need for external debouncing circuitry. If Autorepeat is enabled through QFPro, holding the VUP pin or VDN pin low for approximately two seconds will cause the gain to change repeatedly up or down, as appropriate. Repeatedly toggling the MUTE pin low (default state is high) will alternately mute and un-mute all three channels simultaneously.

An amplifier protection pin, AMP, is provided to aid in the protection of amplifiers that don't have thermal or other protection from very loud signals. At Power-on Reset, this pin is configured with an internal pull-down resistor enabled. If the pin is held high for at least 30 ns, the volume is decreased by 3 dB (default value). Other attenuation values can be programmed as well. The reduced volume will remain until AMP is deasserted.

Volume changes brought about by VUP, VDN, MUTE, or PROF pushbutton presses or their corresponding register accesses will be slew rate controlled to minimize popping sounds. The AMP pin is slew rate controlled as well.

4.11 5-Band Graphic Equalizer, GEQ

The GEQ is a 5-band graphic equalizer that can be controlled by the product's end user. Each of the 5 parallel bands is composed of a 2nd order IIR filter whose gain can be independently varied from +15 dB to –15 dB. Each profile consists of a set of gains (five per profile) for 1 to 8 profiles as established by the developer.

The product's end user can control the GEQ by choosing one of up to eight unique profiles. This is accomplished by either the PROF pin or other interfaces supported by a microcontroller, SPI or SIB bus master, directly setting the internal GEQ registers.

The PROF pin method of controlling frequency response is useful if there is no external microcontroller in the system. Each time the PROF pin is momentarily toggled low, the profile pointer advances to the next profile in a round-robin fashion. The PROF pin is configured similar to the volume pins described above. There is an option for a tone to be generated as the profile pointer advances to the next profile, with a unique pitch signifying the transition from the last profile in the sequence back to the first.

4.12 Dynamic Bass and Treble, DYB/DYT

Dynamic bass compensates for the increased difficulty in hearing bass as the volume is decreased. The DYB block compensate for this by boosting lower frequencies as their energy level or amplitude decreases.

Dynamic treble compensates for the increased difficulty in hearing treble as the volume is decreased. The DYT block will boost the higher frequencies.

Dynamic bass and dynamic treble can be independently enabled and, using QFPro, are highly programmable with respect to operating frequency range and corresponding amplitudes.

4.13 Clipping Control

A user-programmable soft clipper algorithm is available in the QF3DFX. This algorithm applies attenuation to each sample in a non-linear fashion based on that sample's incoming amplitude. After this attenuation, the entire waveform can be gain compensated to create a signal that sounds louder than the original, but with no greater amplitude than the original.

4.14 Crossover

The crossover block will split each staellite channel into two frequency bands by way of a high pass filter and a low pass filter. This allows the user to better match the low and high frequencies to the speakers (e.g. woofers and tweeters). The filters will be in the form of a crossover filter in which each will share the same corner frequency. The block is comprised of eight 2^{nd} order filters capable of many types of crossover structures including the classic Linkwitz-Riley filter with independent gain settings.

4.15 Output Routing and Amplitude

For the I2S or TDM outputs, any of the 5 internal channels (2.2.1; 2.1+ crossover) may be directed to any of the available 6 output I2S channels or 8 TDM slots including directing a single channel to multiple slots and ports.

The amplitude of each the 5 internal channels can be independently set and optionally inverted, allowing for the creation of digital differential outputs.

4.16 Configuration Interface

The Configuration Interface is used to read and write the register and memory spaces. It supports both SIB and SPI protocols. The SIB can function as both a master and a slave. The SPI operates only as a slave. There are 2 address pins available for SIB system requirements.

The Configuration Interface supports self booting (configure and run) from an external SIB-based EEPROM. The EEPROM is also utilized to save user controlled volume and profile setting for reinstatement at power up.

The external SIB EEPROM is a standard 16-bit format device.

The SPI Interface is capable of operating up to 25 MHz, while the I2C interface can run up to 400 kHz. Both interfaces can run with a clock frequency down to DC.

5 CONFIGURATION INTERFACE

The configuration interface consists of a SPI interface and a standard 2-wire interface, referred to in this document as the Serial Interface Bus (SIB), with the following features:

- SIB Interface
  - Pins are cSCL and cSDA and are I2C compatible
  - Both a master and a slave
  - Boot interface that supports a variety of EEPROMs
  - Schmitt trigger input levels are always enabled on the SIB pins
- SPI Interface
  - Slave Only
- SPI to SIB Bridge
  - Can program the SIB EEPROM from a SPI Master
  - Can access any slave device on the SIB from a SPI Master
- Flexible microprocessor support
  - Zero, one, or multiple microprocessors supported
  - Multiple microprocessors may require system (off-chip) arbitration

Figure 5-1 Configuration Dataflow Diagram, is the overall block diagram for the configuration interface. The functionality of the blocks is summarized below.

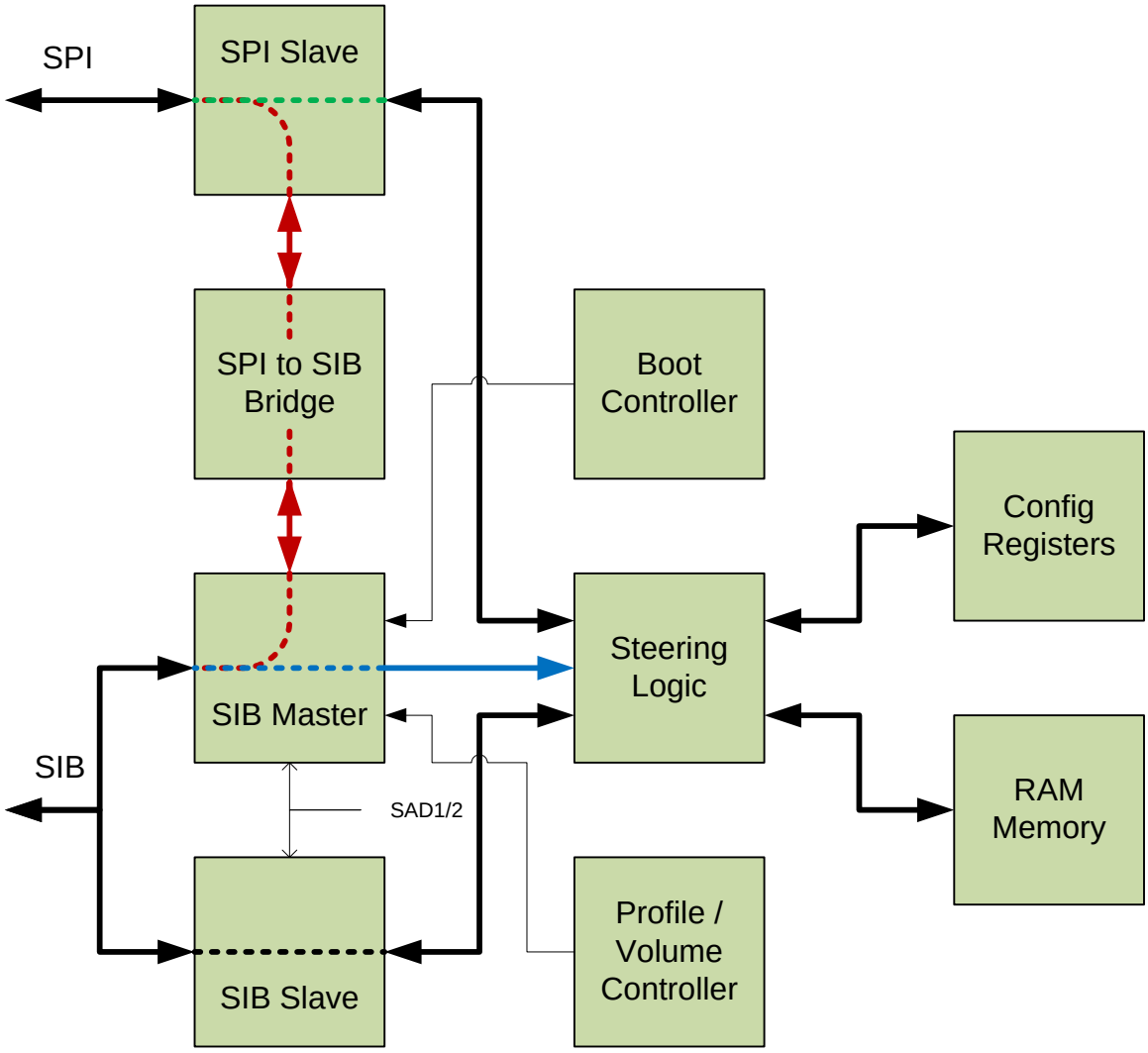


Figure 5-1 Configuration Dataflow Diagram

SPI Slave – Through this interface, an external SPI master can access (read or write) the register space, the memory space, and the SIB bus.

SPI-to-SIB Bridge – This allows an external SPI master to access the SIB bus. Using this bridge is one method in which the system can program the associated SIB EEPROM.

SIB MASTER – Its main purpose is to access an external SIB EEPROM during boot-up. The boot block will, following reset, use the SIB master to access an EEPROM, if one exists. An external SPI master can also use the SIB master to access an SIB-based EEPROM, or any other slave device on the SIB.

SIB SLAVE – The SIB Slave is used by an external SIB master to access (read or write) the register and memory spaces.

BOOT CONTROLLER – This block, following reset, will cause the SIB Master to attempt an access to an external SIB EEPROM. It will check to see if an EEPROM is on the bus and then, via a predefined header format, determine if the data

in the EEPROM is valid for the QF3DFX. If the data is valid, it will then transfer the data from the EEPROM to the register and memory spaces in the QF3DFX.

PROFILE / VOLUME CONTROLLER – This block will update an external SIB EEPROM with current profile and volume information. In an implementation that does not include a microprocessor, this block allows the last settings of the profile and volume to be saved to an external SIB EEPROM.

STEERING LOGIC – This block determines which controller can access (read or write) to the register and memory spaces. The boot block has highest priority, followed by the SPI interface, with the SIB slave interface having the lowest priority.

CONFIG REGISTERS – This block represents the chip's configuration register space.

MEMORIES – This block represents the chip's ram-based memory spaces, holding volume table, coefficient, reserved information, and data information.

The following sections describe each of the blocks and the interface protocol for each.

5.1 Serial Peripheral Interface (SPI) Protocol

5.1.1 Mode of Operation

The QF3DFX is designed to interface directly with the serial peripheral interface (SPI) of microcontrollers and Digital Signal Processors. The QF3DFX SPI slave mode uses the **cSDI**, **cSDO**, **cSCK,** and **cCSn** pins. **cSDI** is the input serial data, and **cSDO** is the output serial data. **cSCK** is the input serial clock. **cCSn** is the SPI peripheral select line. The configuration registers can be both read and written while audio data is being processed. Coefficient and Volume data accesses must not be attempted while audio data is being processed.

5.1.2 Data Format

In order to address and read/write to the QF3DFX, **cCSn** is asserted low to select the device. If **cCSn** is not asserted, data will not be accepted via the serial input pin (**cSDI)** and the serial output pin (**cSDO**) will remain in a high impedance state.

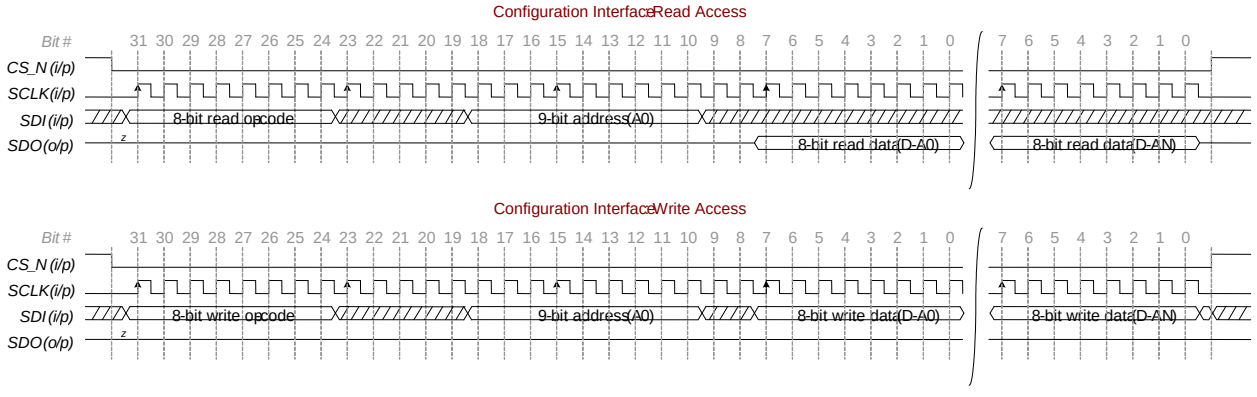


Figure 5-2: Configuration Data Timing

Important Notes

- There are **five** “don’t care” clock cycles between the end of the op code and the 9-bit address. The value of **cSDI** during these clocks has no effect on the chip. There are also **two** “don’t care” clock cycles between the end of the address input and data output on the **cSDO** pin.
- **cSDO** transitions are always based from the falling edge of **cSCK**
- **cSDI** is always sampled on the rising edge of **cSCK**
- **cSDO** is tri-stated when **cCSn** is high
- Holding **cCSn** low continues data read/write accesses
- Read Opcodes: Register Space = 0x83, Reserved Space = 0x85, Coefficient RAM Space = 0x87, Volume RAM Space = 0x92
- Write Opcodes: Register Space = 0x82, Reserved Space = 0x84, Coefficient RAM Space = 0x86, Volume RAM Space = 0x93
- SPI-to-SIB Opcodes: Write SIB = 0x94, Continue Write SIB = 0x95, Read SIB = 0x96, SIB Done = 0x97
- The address for the Configuration Registers is a byte address, e.g. to read the VERSION register, the address would be 0x02.
- The address for the Resereved RAM identifies the reserved location to be accessed, e.g. to write the 4th reserved location directly, the address would be 0x03 [1st resrv addr = 0x00, 2nd resrv addr = 0x01, 3rd resrv addr = 0x02, 4th resrv addr = 0x03]. Each reserved location is six bytes wide. There are 512 coefficient locations resulting in the address being 9 bits wide.
- The address for the Coefficient RAM identifies the coefficient to be accessed, e.g. to write the 4th coefficient directly, the address would be 0x03 [1st coeff addr = 0x00, 2nd coeff addr = 0x01, 3rd coeff addr = 0x02, 4th coeff addr = 0x03]. Each coefficient is three bytes wide. There are 512 coefficient locations resulting in the address being 9 bits wide.
- The address for the Volume RAM identifies a 7-bit gain value to be accessed, e.g. to write the 4th gain value directly, the address would be 0x03 [1st gain value. addr. = 0x00, 2ndgain value addr = 0x01, 3rd gain value addr = 0x02, 4th gain value addr = 0x03]. Each gain value is seven bits wide. There are 100 gain value locations resulting in the address being 7 bits wide.

5.1.3 Address Spaces

The Configuration SPI interface programs four different address spaces in the QF3DFX: a Configuration Register space, a Coefficient Memory space, a Reserved Memory space, and a Volume Memory space. The Configuration Register space is accessed when the Opcodes 0x82/0x83 are used. The Reserved Memory space is accessed when the Opcodes 0x84/0x85 are used. The Coefficient Memory space is accessed when the Opcodes 0x86/0x87 are used. The Volume Memory is accessed when Opcodes 0x92/0x93 are used.

Multiple successive registers or memory values may be read or written by simply appending 8-bit data values after the first data value is read or written. Thus an entire Coefficient, Volume, Configuration Register, or Reserved Memory space may be read or written with a single write access.

Each 48-bit reserved location is written Most Significant Bit and Most Significant Byte first. Each 24-bit coefficient is written Most Significant Bit and Most Significant Byte first. Each 8-bit configuration register is written Most Significant Bit first. Certain configuration values span more than one byte. These get written Least Significant Byte first, but Most Significant Bit first (within a byte). The volume memory only uses the lower 7 bits; therefore, the MSb (Most Significant bit of the byte) is a don’t-care. The table below summarizes this.

Registers	Address Range	Data Size†	Write Opcode	Read Opcode
Configuration Registers	0x00 – 0x9C (0-156)	8 bits	0x82	0x83
Reserved Values	0x00 – 0x1FF (0-511)	48 bits	0x84	0x85
Coefficients	0x00 – 0x1FF (0-511)	24 bits	0x86	0x87
Volume	0x00-0x63 (0-99)	7 bits	0x92	0x93

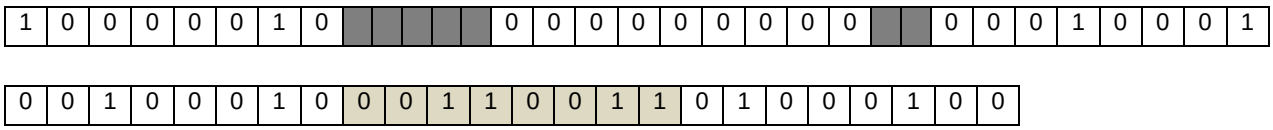
† Multiple registers can be written / read by extending the SPI access cycle

Table 5-1: Register and Memory Access Formats

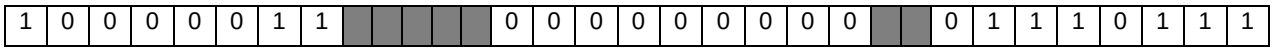
Note: When the Mode Control Register (register 03h) contains a value of one (01h), the QF3DFX is in Filter Mode and the Coefficient, Volume, and Reserved Memory spaces cannot be accessed. In this mode, only the Configuration Registers can be freely accessed. In order to freely read and write any memory space location, the Mode Control Register must be written with a value of zero (00h).

The following are examples of SPI writes and reads to configuration, coefficient, and volume memory spaces.

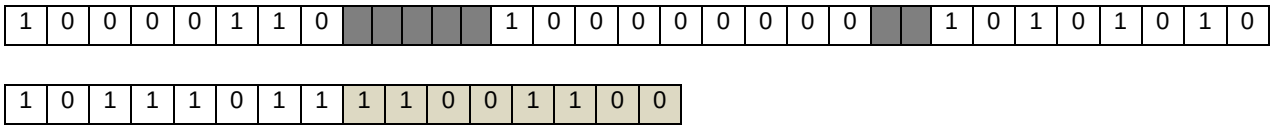
1) SPI write to the first four registers with data of 0x11, 0x22, 0x33 and 0x44.
Bit Stream: 0x82, 0xX (5), 0x000 (9), 0xX (2), 0x11223344



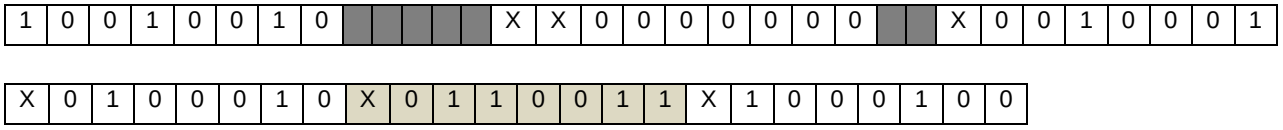
2) SPI read of address 0x00 with data of 77
Bit Stream: 0x83, 0xX (5), 0x000 (9), 0xX (2), Data (received)



3) SPI write to coefficient memory at address 0x100 with data of 0xaabbcc.
Bit Stream: 0x86, 0xX (5), 0x100 (9), 0xX (2), 0xaabbcc

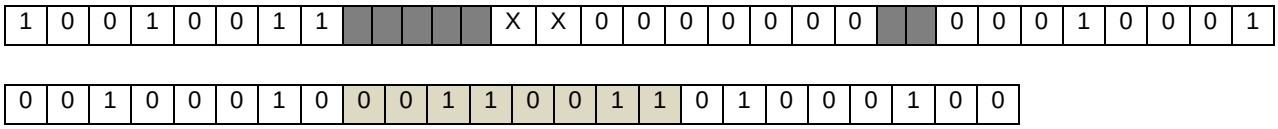


4) SPI write to the first four volume memory locations with data of 0x11, 0x22, 0x33 and 0x44.
Bit Stream: 0x92, 0xX (5), 0x000 (9), 0xX (2), 0x11223344



5) SPI read of the first four volume memory locations with data of 0x11, 0x22, 0x33 and 0x44.

Bit Stream: 0x92, 0xX (5), 0x000 (9), 0xX (2), 0x11223344. Note that the Most Significant Bit is always returned as 0.



5.1.4 SPI Access to EEPROM

The SPI interface can read and write an external SIB EEPROM. Several Opcodes are used to accomplish this: 0x94 through 0x97. Opcode 0x94 sent from the external SPI master initiates a write to the SIB bus. This write can only have one byte of data. The external SPI master must then poll the SPI_TO_I2C status register to see when it may begin the next write. Typically, the SPI will be able to keep data flowing uninterrupted to the SIB bus. A second Opcode, 0x95, is provided in order to allow the external SPI master to issue a write command without the need for address information. A third Opcode, 0x96, is provided to do a single byte read from the EEPROM. A fourth Opcode, 0x97, will end the write (either due to reaching a page boundary in the EEPROM or on the completion of the EEPROM access). The Opcodes are summarized in the following table.

Access Type	Data Size	Opcode
SPI to SIB Write	8 bits	0x94
SPI to SIB continued Write	8 bits	0x95
SPI to SIB Read	8 bits	0x96
SPI to SIB Done	N/A	0x97

Table 5-2: SPI-to-SIB Accesses

The following table shows the information that the SPI Master must provide for each of the four Opcodes.

Access Type	Information
SPI to SIB Write	Opcode, Device Address, Internal Address High, Internal Address Low, Data
SPI to SIB continued Write	Opcode, Data
SPI to SIB Read	Opcode, Device Address, Internal Address High, Internal Address Low
SPI to SIB Done	Opcode, Device Address

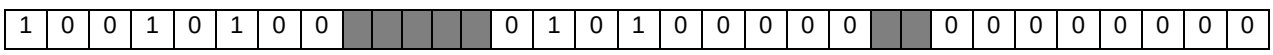
Table 5-3: SPI-to-SIB Accesses

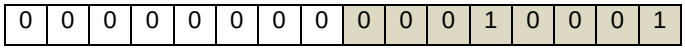
Example 1

This example of a SPI to SIB write assumes an EEPROM with a Device Address = 0xA0. The write will begin at the EEPROM address of 0x0 and write four bytes: 0x11, 0x22, 0x33, and 0x44.

1) To initiate the write the SPI Master would write out the following information (in the manner as shown in Figure 5-2: Configuration Data Timing).

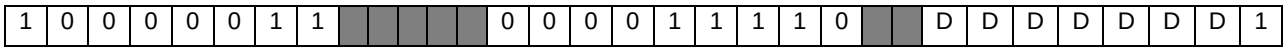
   a. 0x94, 0xX, 0x0A0, 0xX, 0x0, 0x0, 0x11 (8-bit opcode, 5 don't cares, 9-bit address, 2 don't cares, 8-bit internal address high, 8-bit internal address low, 8-bit data)





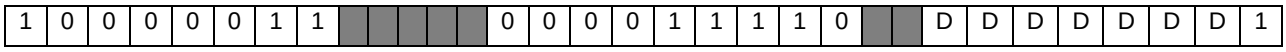
2) The SPI Master must now poll the SPI_TO_SIB register bit 0, which when set indicates that the SIB write is complete

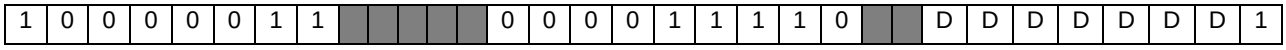
   a. 0x83, 0xX, 0x1e, 0xX, 0xXd (8-bit opcode, 5 don't cares, 9-bit address, 2 don't cares, 8-bit received data)

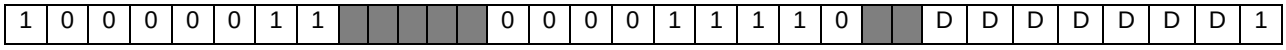


3) To continue on with the remaining three bytes

   a. 0x95, 0xX, 0x22 (8-bit opcode, 5 don't cares, 8-bit data)
   b. 0x83, 0xX, 0x1e, 0xX, 0xXd (8-bit opcode, 5 don't cares, register address, 2 don't cares, received data)
   c. 0x95, 0xX, 0x33 (8-bit opcode, 5 don't cares, 8-bit data)
   d. 0x83, 0xX, 0x1e, 0xX, 0xXd (8-bit opcode, 5 don't cares, register address, 2 don't cares, received data)
   e. 0x95, 0xX, 0x44 (8-bit opcode, 5 don't cares, 8-bit data)
   f. 0x83, 0xX, 0x1e, 0xX, 0xXd (8-bit opcode, 5 don't cares, register address, 2 don't cares, received data)







4) To end the transfer

   a. 0x97, 0xX, 0xXX, 0xX (8-bit opcode, 5 don't cares, 9 don't cares, 2 don't cares)

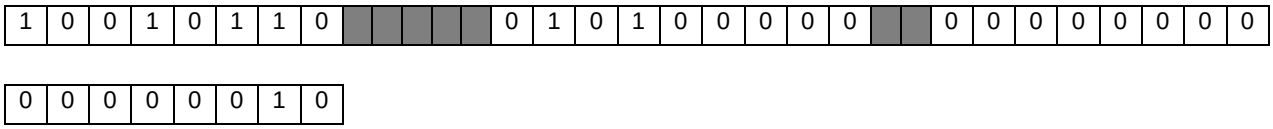
   Note: the value after the opcode is a don't-care, but for proper operation there must be a 16-bit value following the opcode.

Example 2

This example of a SPI to SIB read assumes an EEPROM with a device address of 0xA0. The data at the EEPROM address 0x2 (data = 0x46) is being read by a SPI master

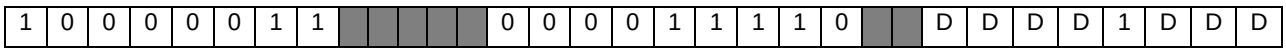
1) The SPI master begins a read to the SIB EEPROM

   a. 0x96, 0xX, 0x0A0, 0xX, 0x0, 0x2 (8-bit opcode, 5 don't cares, 9-bit address, 2 don't cares, 8-bit address high, 8-bit address low)



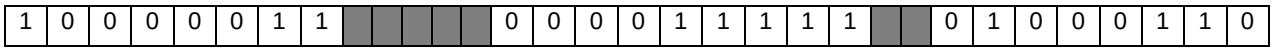
2) The SPI Master must now poll the SPI_TO_SIB register bit 3, which, when set, indicates that the SIB read is complete.

   a. 0x83, 0xX, 0x1E, 0xX, 0XD (8-bit opcode, 5 don't cares, 9-bit register address, 2 don't cares, received data)



3) The SPI Master can read the SIB data register in which the requested byte of EEPROM data will be located.

   a. 0x83, 0xX, 0x1F, 0xX, 0xD (8-bit opcode, 5 don't cares, 9-bit register address, 2 don't cares, received data)



5.2 SIB Slave

The QF3DFX SIB Slave interface can access the Configuration Registers and the Coefficient, Reserved, and Volume Memory spaces. The SIB Slave interface uses several opcodes to accomplish writes and reads.

Following boot and until the internal initialization is complete, the SIB Slave interface will not allow an external master access to the Configuration Registers or to the memories. The slave will return a no acknowledge during the device address phase. Table 5-4: SIB Slave Opcodes lists the opcode for each type of slave access.

Registers	Address Range	Data Size	Read/Write Opcode
Configuration Registers	0x00 – 0x77 (0-119)	8 bits	0x82
Reserved Memory	0x00 – 0x1FF (0-511)	48 bits	0x84
Coefficients Memory	0x00 – 0x1FF (0-511)	24 bits	0x86
Volume Memory	0x00 – 0x63 (0-99)	7 bits	0x92

Table 5-4: SIB Slave Opcodes

The SIB master must begin an access (either read or write) with the device address. The device address for the QF3DFX SIB slave is a combination of the hard coded value of 0xc0, the value of two external pins SAD1 and SAD2, and the Read/Write bit. The results in the slave address equaling:

1	1	0	0	0	SAD2	SAD1	R/W

After the device address has been sent, the SIB master must send the opcode (see Table 5-4: SIB Slave Opcodes). Following the opcode, the 2-byte address for the internal destination in QF3DFX (register or memory address) is sent. The upper byte (first one sent) will be all zeros for register accesses and for volume memory accesses. The Coefficient Memory and the Reserved Memory will use the least significant bit of the upper byte. Following the address, the SIB master sends the data. The data is in byte format with the most significant byte first. Below are some examples.

Note: ACK = Acknowledge, NAK = No Acknowledge, RST = Restart (the START and STOP conditions are not shown)

Example 1: An external SIB Master write to configuration register 0x00 with a data of 0x55.

SAD2 = SAD1 = 0

STR	1	1	0	0	0	0	0	R/W 0	ACK	1	0	0	0	0	0	1	0	ACK	0	0	0	0	0	0	0	0	ACK	0	0	0	0	0	0	0	0	ACK

0	1	0	1	0	1	0	1	NAK	STP

Example 2: An external SIB Master read to configuration register 0x06 with expected data of 0xAA.

SAD2 = SAD1 = 1

STR	1	1	0	0	0	1	1	R/W 0	ACK	1	0	0	0	0	0	1	0	ACK	0	0	0	0	0	0	0	0	ACK	0	0	0	0	0	1	1	0	ACK

RST	1	1	0	0	0	1	1	R/W 1	ACK	1	0	1	0	1	0	1	0	NAK	STP

Example 3: An external SIB Master write to coefficient memory address 0x111 with data of 0x112233

SAD2 = SAD1 = 0

STR	1	1	0	0	0	0	0	R/W 0	ACK	1	0	0	0	0	1	1	0	ACK	0	0	0	0	0	0	0	1	ACK	0	0	0	1	0	0	0	1	ACK

0	0	0	1	0	0	0	1	ACK	0	0	1	0	0	0	1	0	ACK	0	0	1	1	0	0	1	1	NAK	STP

Example 4: An external SIB Master read to coefficient memory address 0x113 with expected data of 0x112233

SAD2 = SAD1 = 0

S T R	1	1	0	0	0	0	0	R/W 0	A C K	1	0	0	0	0	1	1	0	A C K	0	0	0	0	0	0	0	1	A C K	0	0	0	1	0	0	1	1	A C K

R S T	1	1	0	0	0	0	0	R/W 1	A C K	0	0	0	1	0	0	0	1	A C K	0	0	1	0	0	0	1	0	A C K	0	0	1	1	0	0	1	1	N A K	S T P

Example 5: An external SIB Master write to volume memory address 0x023 with data of 0x66

SAD2 = SAD1 = 0

S T R	1	1	0	0	0	0	0	R/W 0	A C K	1	0	0	1	0	0	1	0	A C K	0	0	0	0	0	0	0	0	A C K	0	0	1	0	0	0	1	1	A C K

X	1	1	0	0	1	1	0	N A K	S T P

Example 6: An external SIB Master read from volume memory address 0x043 with expected data of 0x4C

SAD2 = SAD1 = 0

S T R	1	1	0	0	0	0	0	R/W 0	A C K	1	0	0	1	0	0	1	0	A C K	0	0	0	0	0	0	0	0	A C K	0	1	0	0	0	0	1	1	A C K

R S T	1	1	0	0	0	0	0	R/W 1	A C K	0	1	0	0	1	1	0	0	N A K	S T P

The Data Length of each access is dependent on its intended location. An access to the register space or the volume space is a 1-byte access; an access to coefficient space is a 3-byte access; an access to the reserved space is a 6-byte access. If an access that is not the exact size occurs, then the QF3DFX SIB slave state machine will hang. It expects the exact number of bytes. Table 5-5 - Access Size, lists the byte size per access.

Access	Access Size
Configuration Registers	1 byte (8 bits)
Coefficient Memory	3 bytes (24 bits)
Volume Memory	1 byte (7 bits)
Reserved Memory	6 bytes (48 bits)

Table 5-5 - Access Size

The length of the data access can be as long as the entire range of the register or memory map. It can be any size as long as it follows the access size rule. As an example, a write to coefficient memory can be any multiple of 3 bytes (i.e. 3, 6, 9, 12, 15, etc). It cannot be 4 bytes long. A write to register space or to volume memory can be 1, 2, 3, 4, 5 … number of bytes long.

5.3 SIB Master/Boot

5.3.1 Introduction

The QF3DFX SIB Master has two functions:

- Access an external EEPROM during boot
- Complete a write or read from an external SPI master to an SIB slave device, primarily a EEPROM.

The Auto Loader can be used in place of a microcontroller to load a configuration (registers, reserved locations, coefficients, and volume) into the QF3DFX chip. The Auto Loader has the ability to detect if there is an EEPROM present or not. Once the EEPROM has been detected, the Auto Loader will do an atomic transfer of all the data.

An external SPI Master can access an external SIB EEPROM. This is described in detail in section 5.1, Serial Peripheral Interface (SPI) Protocol.

5.3.2 Auto Loader Features

- Atomically reads all of the data from the EEPROM and transfers it to the appropriate registers and coefficient memory locations.
- Supports standard EEPROM16-bit addressing mode.
- Externally selectable primary target address of 0x50, 0x51, 0x52, and 0x53 (note: these device addresses are 7-bits wide, bit zero (LSb) of the actual 8-bit SIB address phase transfer is the read/write bit).
- Detects valid EEPROM device on bus and authenticates the QFT header contents prior to loading data.
- Supports loading data from any location based on starting address as loaded in the EEPROM header.
- Supports page turn and end-load instructions.

IMPORTANT: The SIB Master is not able to detect collisions with other SIB Masters during the Auto Load sequence. Because of this, multiple QF3DFX chips that sit on the same two SIB wires must be brought out of the reset individually and separated in time. Once the first QF3DFX is brought out of reset, the other QF3DFX chips (and any other SIB masters) must not be brought out of reset until the first QF3DFX has completed the Auto Load sequence. Bit 5 of the BOOT_STATUS register in the first QF3DFX chip will be set when it is done Auto Loading. Additional QF3DFX chips may then be brought out of reset in a similar fashion.

5.3.3 Supported EEPROM Characteristics:

- Supported EEPROMs include only devices that use 16-bit addressing. An example is the Microchip M24LC128 family.
- Fixed page/block sizes of 256 bytes for EEPROMs that require a new transfer on page boundaries for reads.
- The 16-bit type device addressing format consists of one EEPROM with multiple pages of 256 bytes at a single SIB address (some EEPROMs do not require paging for reads). A single 16-bit EEPROM can also be used by up to four QF3DFXs by using the SAD1 and SAD2 pins.
- Page turns are accomplished by changing the upper byte of the 16-bit address while the SIB address remains constant through entire address range.
- The device must have a base starting SIB address that is configurable to 0x50 through 0x53 (This is the unshifted, 7-bit address, where the four most significant bits are 1010b). A QF3DFX can access up to four devices by using the SAD1 and SAD2 pins to program the two LSB bits in the device address. The start address in the header or Page-turn instruction can point to a different page that is anywhere from 0x50 to 0x57 (Only the offset from 0 to 7 needs to be specified).
- SIB data bus speed should be limited to a maximum 400 kHz operation to facilitate slow cheap EEPROMs.

The reader must consult the EPPROM manufacturers' data sheets for complete details and correct timing information.

5.3.4 EEPROM Access Flow

The flow chart in Figure 2, Auto Loader Flow Chart, indicates the basic flow of the Auto Loader.

After reset, if enabled, the Auto Loader will arbitrate for the bus by writing out the slave address. If the Auto Loader is not granted the bus, it will continue to try until access is granted.

Once granted access, the Auto Loader will follow the slave address with an attempt to read portions of the header field of the EEPROM. The Auto Loader will compare locations 0x00, 0x01, and 0x02 to their expected contents ('Q', 'F', and 'T') and will compare the checksum at location 0x0F with its own calculation using the data from locations 0x00 – 0x06.

If the header information is found to be valid, then the Auto Loader will begin to read the EEPROM. Multiple atomic reads will continue until the EEPROM sends an instruction to begin on a new page or the EEPROM sends an instruction to end the access. If the instruction is a page-turn then the Auto Loader will begin the access by writing out the slave address followed by the new word address (the header reads do not repeat). If the instruction is a done-instruction then the auto reader will end the access and turn off until the next reset.

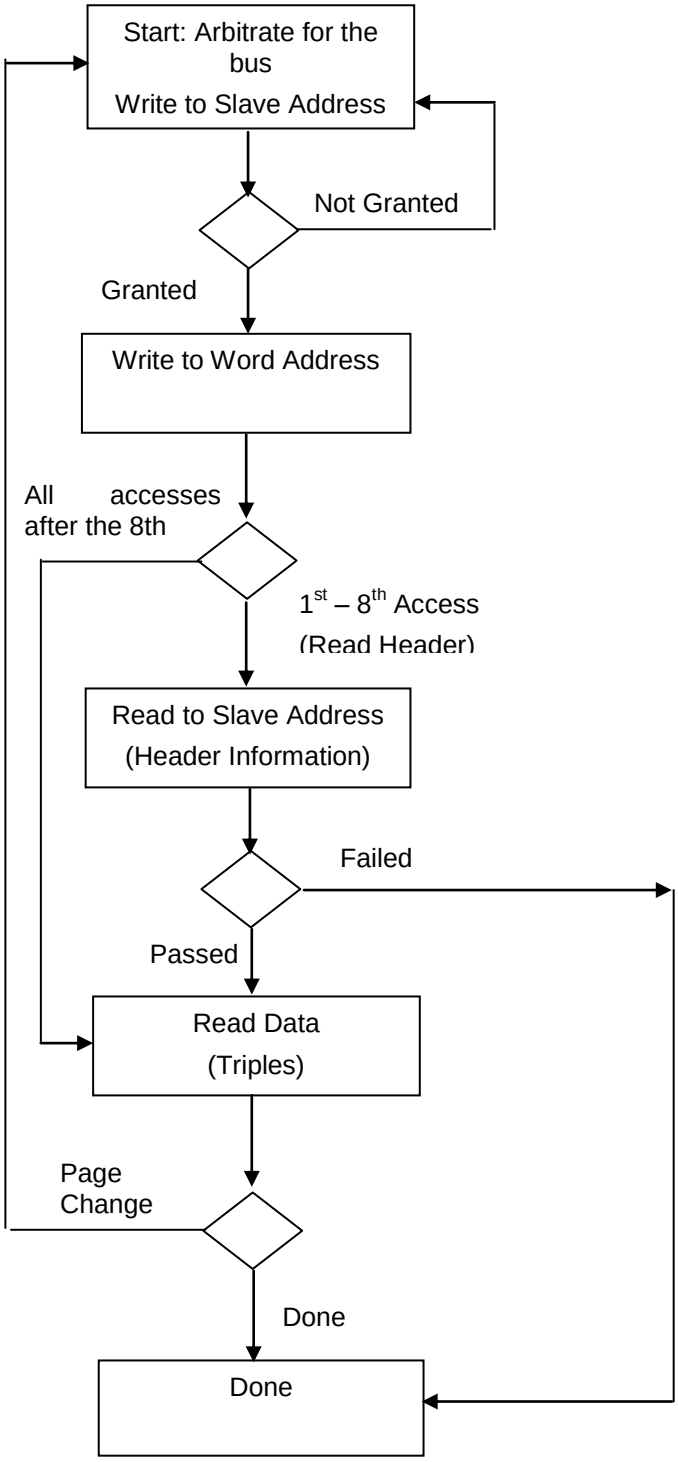


Figure 5-2: Auto Loader Flow Chart

5.3.5 EEPROM Header Format

Prior to importing data from an EEPROM, the contents are authenticated to ensure that the information in the EEPROM is valid. The authentication method ensures that the first three registers in the header contain the ASCII characters “QFT” and the last register contains a zero checksum calculated on the first 7 registers in the header.

The Auto Loader expects to find the EEPROM header beginning at the base location of an EEPROM located at either 0x50, 0x51, 0x52, or 0x53. The EEPROM header registers are always located starting at address 0x00 in the first page of EEPROM memory for address 0x50. The header information for the other addresses are located at an offset of 4k byte. The main purpose of this is to allow up to four QF3DFXs to share one EEPROM. The EEPROM starting address location for an address of 0x51 would be 0x800, for 0x52 it would be 0x1000, for 0x53 it would be 0x1800.

Address	Name	Description	Value
00	IDENQ	Contains the ASCII character “Q” as in **Q**uickfilter	0x51
01	IDENF	Contains the ASCII character “F” as in Quick**F**ilter	0x46
02	IDENT	Contains the ASCII character “T” as in **T**echnologies	0x54
03	ECFG	EEPROM Configuration • B7 is addressing type for memories • B6 is reserved • B5:0 contains page number of last location used	User Set
04-12	SAMSB	Starting Address of Most Significant Byte	User Set
05-13	SALSB	Starting Address of Least Significant Byte	User Set
14	REVNUM	Revision number of EEPROM Image • B7:4 is major revision number • B3:0 is minor revision number	User Set
15	EHCS	EEPROM Header zero check sum of registers 0x0 – 0x6	Calculated

Table 5-6: EEPROM Header Register Map

Identification Q Register **Address 0h**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	0	1	0	1	0	0	0	1
Mnemonic	IDENA(7:0)							
Access	RO	RO	RO	RO	RO	RO	RO	RO

Mnemonic	Description
IDENA	Contains the ACSII character “Q” Must be properly decoded by the loader to continue

Identification F Register — Address 1h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	0	1	0	0	0	1	1	0
Mnemonic	IDENT(7:0)							
Access	RO	RO	RO	RO	RO	RO	RO	RO

Mnemonic	Description
IDENT	Contains the ACSII character “F” Must be properly decoded by the loader to continue

Identification T Register — Address 2h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	0	1	0	1	0	1	0	0
Mnemonic	IDENI(7:0)							
Access	RO	RO	RO	RO	RO	RO	RO	RO

Mnemonic	Description
IDENI	Contains the ACSII character “T” Must be properly decoded by the loader to continue

EEPROM Configuration Register — Address 3h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	User Set							
Mnemonic	AT	RSVD	LPU(5:0)					
Access	RW	RW	RW	RW	RW	RW	RW	RW

Mnemonic	Description
AT	Addressing Type 1 = 16 bit Addressing mode. SIB must broadcast full address 0 = 8 bit Addressing mode. SIB broadcasts only 8 bit address
RSVD	Reserved. Returns 0 by default.

Starting Address MSB Register — Address even 4h-12h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	User Set							
Mnemonic	SAMSB(7:0)							
Access	RW	RW	RW	RW	RW	RW	RW	RW

Mnemonic	Description
SAMSB	Contains the Starting Address MSB of the QF3DFX data. MSB in 16 bit addressing mode is used to access the appropriate memory page. For 8 bit addressing mode, it would be used to access the correct device by adding the value in this register to the initial device address of 0x50. For 8 bit device, the valid range is 0x00 to 0x07.There eight of these registers in each QF3DFX, but only one is used. The correct register for an individual QF3DFX is dependent on the state of the Slave address pins. A Slave Address of 000 would correspond to register 4h, A Slave Address of 111 would correspond to register 12h.

Starting Address LSB Register — Address 5h-13h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	User Set							
Mnemonic	SALSB(7:0)							
Access	RW	RW	RW	RW	RW	RW	RW	RW

Mnemonic	Description
SALSB	Contains the Starting Address LSB of the QF3DFX data. Normally the data will be found starting immediately after the EEPROM header. There eight of these registers in each QF3DFX, but only one is used. The correct register for an individual QF3DFX is dependent on the state of the Slave address pins. A Slave Address of 000 would correspond to register 5h, A Slave Address of 111 would correspond to register 13h.

EEPROM Image Data Revision Register — Address 14h

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	User Set							
Mnemonic	MJRRN(3:0)				MNRRN(3:0)			
Access	RW	RW	RW	RW	RW	RW	RW	RW

Mnemonic	Description
MJRRN	Major Revision Number. These four bits are used to ID the image major revision. Unused by HW loader These bits are only used as part of the checksum calculation and are not accessible.

MNRRN	Minor Revision Number. These four bits are used to ID the image minor revision. Unused by HW loader These bits are only used as part of the checksum calculation and are not accessible.

EEPROM Header Checksum Register **Address 15h**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Value	User Set							
Mnemonic	EHCS(7:0)							
Access	RW	RW	RW	RW	RW	RW	RW	RW

Mnemonic	Description
EHCS	Contains the value required to zero check sum, the EEPROM header data contained in registers 0x0 – 0x14. The value contained in this register should result in a sum equal to 0xX00 when added to the above header registers. If this occurs then the data load process will begin at the SAMSB\SALSB location. If no match occurs then the error flag will be set. The auto load will terminate.

5.3.6 Data Format

Except for the header, all data in the EEPROM is aligned in groups of bytes called instructions. Instructions are broken down into several fields always beginning with an 8-bit opcode. The type of transfer is based on the opcode, as shown in the following table.

Data Triple	Name	Description of Triple	YY value
82,yy,yy,zz,zz,data	DRA	Direct Register Addressing mode in QFT devices • YY starting address (first register to be programmed) • ZZ the number of registers to be programmed • The data field is one or more 8-bit register data	0x0000-0x01FF
86,yy,yy,zz,zz,data	CMA	Coefficient Memory Addressing Mode Format • YY is the starting address in coefficient memory • ZZ is the number bytes of coefficient data to be read • The data field is one or more 24-bit memory data in three 8-bit increments	0x0000-0x01FF
FA,zz	PTI	Page turn instruction Mode Format • Operands zz = 0x00 – 0xFE are jump to page zz and operand 0xFF is jump to next page	N.A.
FF,FF	SDL	Stop Data Load (normal termination mode)	X

Table 5-7: EEPROM Instruction Formats

5.3.7 Direct Register Addressing mode

Direct Register Addressing mode directs the data in the EEPROM to one or more of the configuration registers. The first byte is the opcode, which indicates an access to the configuration registers. The second byte (yy) and the third byte (yy) delineate the starting address of the first register to be programmed. The fourth byte (zz) and fifth byte (zz) call out how many registers after the register indicated by the second byte will also be loaded. The subsequent bytes contain the data for the registers. The number of data bytes must match the number indicated in the fourth and fifth bytes.

Register Examples:

82,00,00,00,01,AA indicates the register zero will be programmed to a value of 0xAA.

82,00,00,00,10,AA,BB,CC, … 23 indicates the register zero will be programmed along with the next 16 registers. Register 0 will be programmed to AA, register 1 to BB, … register 15 to 0x23.

82,00,01,00,01,33 indicates that register one will be programmed to a value of 0x33.

82,00,01,00,08,11,22,33, … ,88 indicates the register one will be programmed along with the next seven registers. Register 0 will be programmed to 0x11, register 2 to 22, … , register 7 to 0x88.

5.3.8 Coefficient Addressing Mode Format

Coefficient Addressing Mode directs data from the EEPROM to one or more coefficient memory locations. The first byte is the opcode. The second and third bytes are the starting address. The fourth and fifth bytes are the number of bytes of coefficient data to be read (3 bytes per coefficient). The coefficient memory is three bytes wide, which means that the smallest value for the combination fourth and fifth bytes would be 0x03.

Coefficient Memory Examples:

86,00,00,00,03,11,22,33 indicates that the coefficient memory location 0 will be programmed with a value of 0x112233.

86,00,00,00,09,11,22,33, … ,99 indicates that the coefficient memory location 0 will be programmed along the next 2 locations. This is a total of three memory locations: location 0 = 0x112233, location 1 = 0x445566, location 2 = 0x778899.

86,00,01,00,0C,11,22,33, …, CC indicates that the coefficient memory location 1 will be programmed along with the next 3 locations. This is a total of four memory locations: location 1 =0x112233, location 2 = 445566, location 3 = 778899, location 4 = AABBCC.

5.3.9 Page turn instruction

A page turn will jump to the next 256-byte boundary or to the page directed as defined by zz.

5.3.10 Stop Data Load (normal termination mode)

This command will instruct the QF3DFX SIB master to initiate a Stop Command on the SIB bus.

5.3.11 Status Register

The BOOT_STATUS register is the only configuration register related to the Auto Loader. It is a status register that gives the status of the auto loading. It is a read only register.

6 DATA INTERFACE PROTOCOL

6.1 Introduction

The Data Formatter block handles serial / parallel conversion protocols for the input and output data streams.

On the input side, the Data Formatter will create the parallel data samples from the incoming serial stream on dSDI and separate them into left and right channels as appropriate. It will then present the samples to the Datapath Blocks for processing.

On the output side, the Data Formatter receives samples from up to five data streams coming from the Datapath Blocks and will apply them to the appropriate dSDOn serial streams as programmed.

6.2 Modes of Operation

The QF3DFX is designed to interface directly with a variety of Signal Processing Sources and Sinks. It supports I2S, Left Justified, Right Justified, and TDM serial protocols.

The QF3DFX is designed to work with data widths of 16 and 24 bits.

The QF3DFX supports both 2's complement and offset binary data formats. Data is always transmitted Most Significant Bit first.

6.2.1 I2S, Left-Justified, Right-Justified

Below is a table matching the Data Interface related pins with their functions and I2S names.

Pin Name	Function	I2S Name
dSDI	Serial Data Input	**SD (in)**
dSDO1/2/3	Serial Data Out	**SD (out)**
dCS	Framing Signal	**WS**
dSCK	Serial Clock	**SCK**

Table 6-1 - Pin Names to I2S Names

The **dCS** input indicates which of two (usually left / right) time-division multiplexed data channels is being transmitted. The channels are transmitted alternately on the input data line (**SD** on the **dSDI** input) and are synchronized by a clock line (**SCK** on the **dSCK** input).

The three data protocols (I2S, Left Justified, and Right Justified) are determined by programming the **dsize** and **mode** bits in the DCONFIG register and the **hfs** bits in the HFRAME_SIZE register. For these protocols, the dCS period in dSCK clocks (frame size) must be known and stable. The dCS high time must be the same as the dCS low time. The Data Size must not exceed ½ the frame size (the number of clocks between successive rising or successive falling dCS (WS) edges. Below is a table explaining how the Data Offset and Data Size relate to the protocol.

Protocol	**Start of Frame**	**Fixed Data Offset from Start of Frame (clocks)**	**Data_Size (bits)**
I2S	dCS Falling	1	16/24
Left-Justified	dCS Rising	0	16/24
Right-Justified	dCS Rising	Slot Size – Data Size	16/24

In Figure 6-1 below, all three examples have a frame size of 56 clocks; HFRAME_SIZE must be set to half that, or 28 decimal. All three examples have a data size of 24 bits.

- The I2S Mode example has a fixed data offset of 1 clock from dCS falling and from dCS rising. The frame begins with dCS falling.
- The Left-Justified Mode example has a fixed data offset of 0 clocks from dCS rising and from dCS falling. The frame begins with dCS rising.
- The Right-Justified Mode example has a fixed data offset of 28-24=4 clocks from dCS rising and from dCS falling. The frame begins with dCS rising.

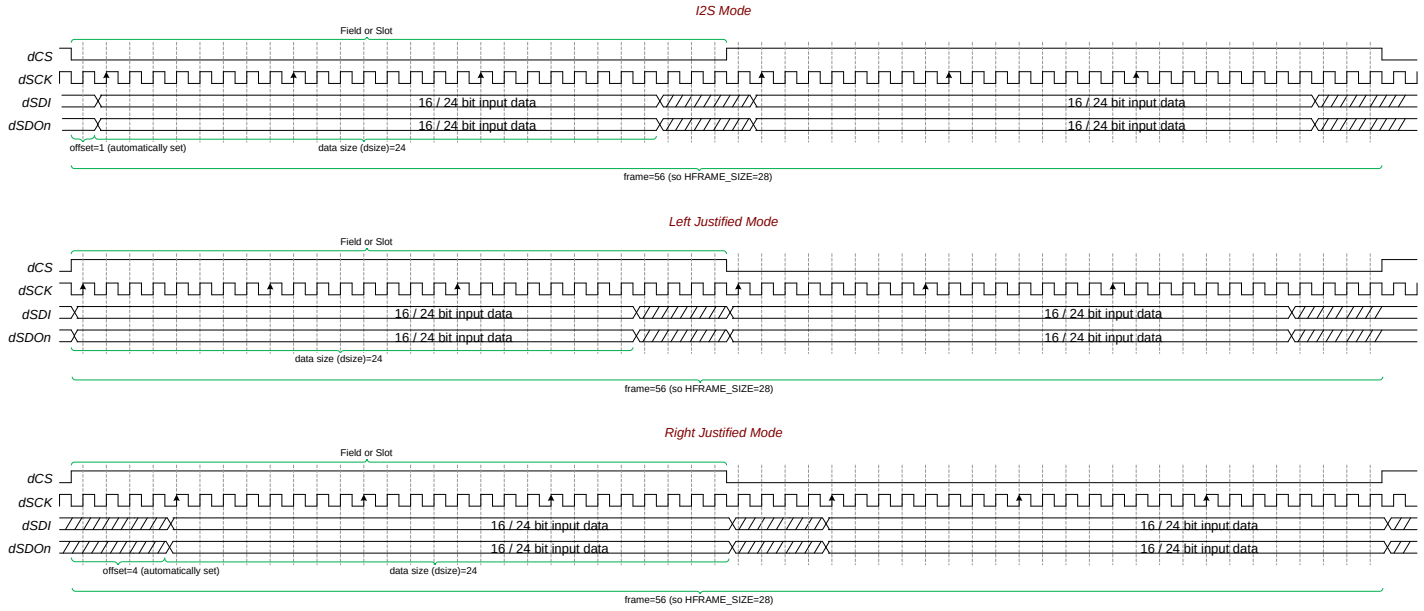


Figure 6-1: Data Interface Timing Diagram I2S/LJ/RJ

The QF3DFX always drives out data from the opposite clock edge that the data is sampled on.

The default operation is to capture data on the rising edge of **dSCK** and drive data on the falling edge of **dSCK** (also known as **SCK**), but this can be changed to capture on falling edge (and drive from the rising edge) by writing the **DCLK_POL** bit in the **DCONFIG** register.

The QF3DFX supports data widths of 16 and 24 bits.

The **FILT_EN** bit must be set to '1' in the **CONTROL** register to enable audio processing. The output stream on the **dSDOn** pin(s) will have the same format as the input stream coming in on the **dSDI** pin.

6.2.2 TDM Mode

TDM (Time Division Multiplexed) Mode is a serial protocol where more than two channels can be placed onto a single wire. A frame (set of samples corresponding to a single point in time) is typically composed of 256 bit-clocks. These clocks are broken into eight groups called slots, each slot consisting of 32 clocks. A data sample sits somewhere within each slot. In TDM Mode, only dSDO1 is used; dSDO2 and dSDO3 are held low.

TDM uses either the rising or falling edge of the framing signal, dCS, to indicate the start of a frame of TDM data. The active edge of dCS is determined by the **dcs_pol** bit in the DCONFIG register. Because only a single edge is used to determine the start of a frame, the dCS signal can be any integral number of bit-clocks wide, from 1 to (frame_length-1).

The HFRAME_SIZE register determines how many clocks are in the frame.

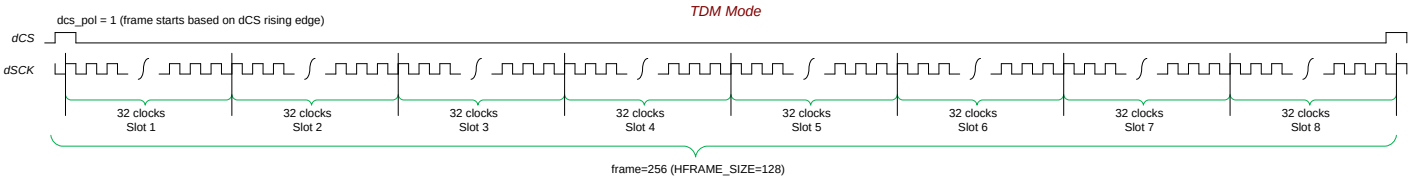


Figure 6-2 - TDM Mode Timing, All Slots

Each data sample sits within a slot. The offset from the start of the slot to the start of the data is determined by the OFFSET1-8 registers; the register name indicating which slot it will provide an offset for. Below are three examples showing timing for Slot 1 (requiring the OFFSET1 register to be set as shown).

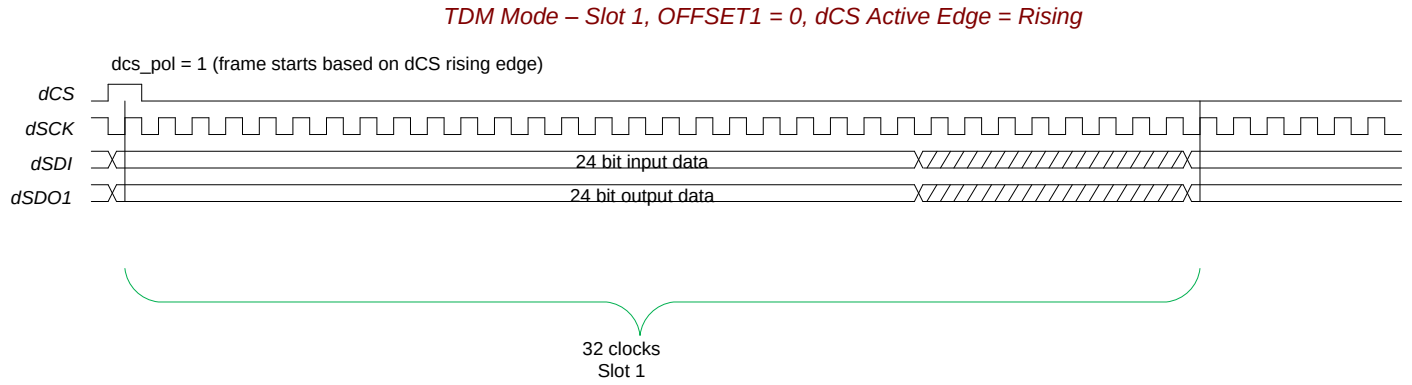


Figure 6-3 - TDM Mode Timing, Slot 1, Offset=0

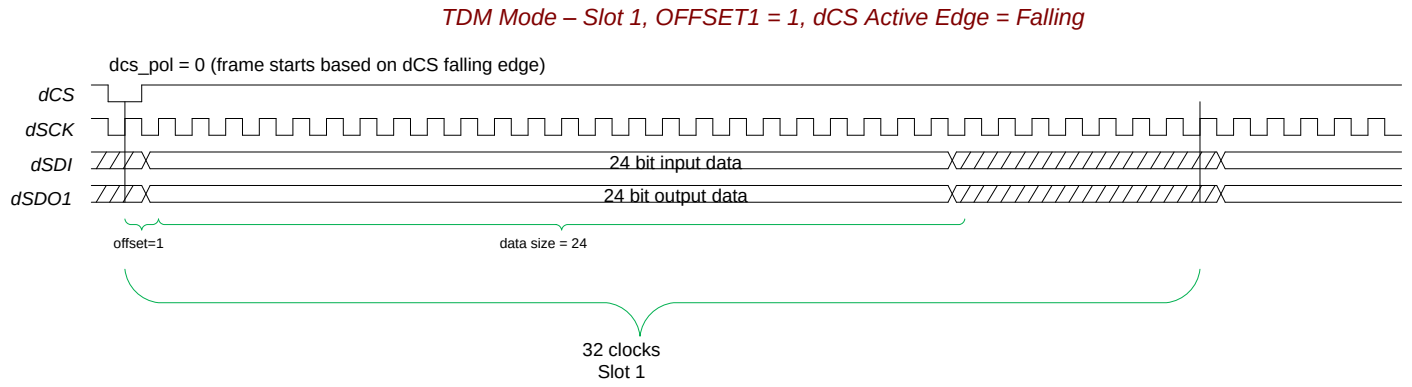


Figure 6-4 - TDM Mode Timing, Slot 1, Offset=1

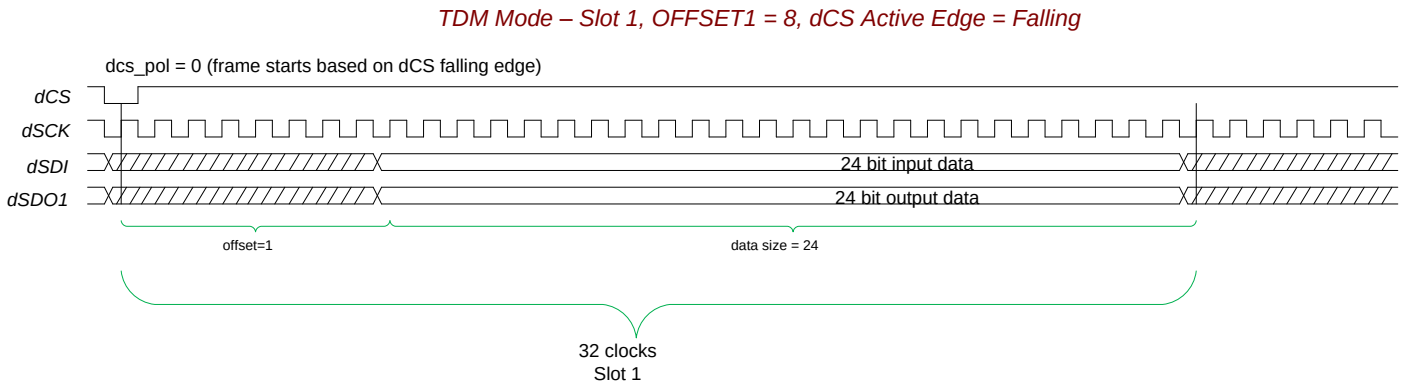


Figure 6-5 - TDM Mode Timing, Slot 1, Offset=8

Each succeeding OFFSETn register must contain the sum of the Slots before it plus the offset of the data sample within its own Slot.

With the flexibility of the OFFSETn and HFRAME_SIZE registers, non-standard TDM protocols can be supported (Frame Sizes that aren't equal to 256 or Slot Sizes that aren't 32-bits long).

The **pass_thru** bit in the DCONFIG register controls dSDO1 behavior during all bits when it is not driving Slot data generated by the QF3DFX chip. If it is a zero, dSDO1 tristates during this time. If it is a one, dSDO1 will asynchronously pass through whatever is on dSDI. This permits devices or channels not processed by the QF3DFX to have data passed along on the TDM bus, even though the QF3DFX isn't directly involved in the signal processing. Care must be taken that overall system timing is still met.

6.3 Input Mixer

All of the input channels / slots are able to contribute to each of the three internal audio channels (2 satellites, 1 SW/Ce). The very first stage of the QF3DFX signal processing path creates a weighted sum for each of the three internal audio channels. Each weighted sum is created by multiplying each input channel / slot by a unique constant value, and then summing all of them. QFPro provides easy assignment of all of these constants. Refer to the figure below for a pictorial representation.

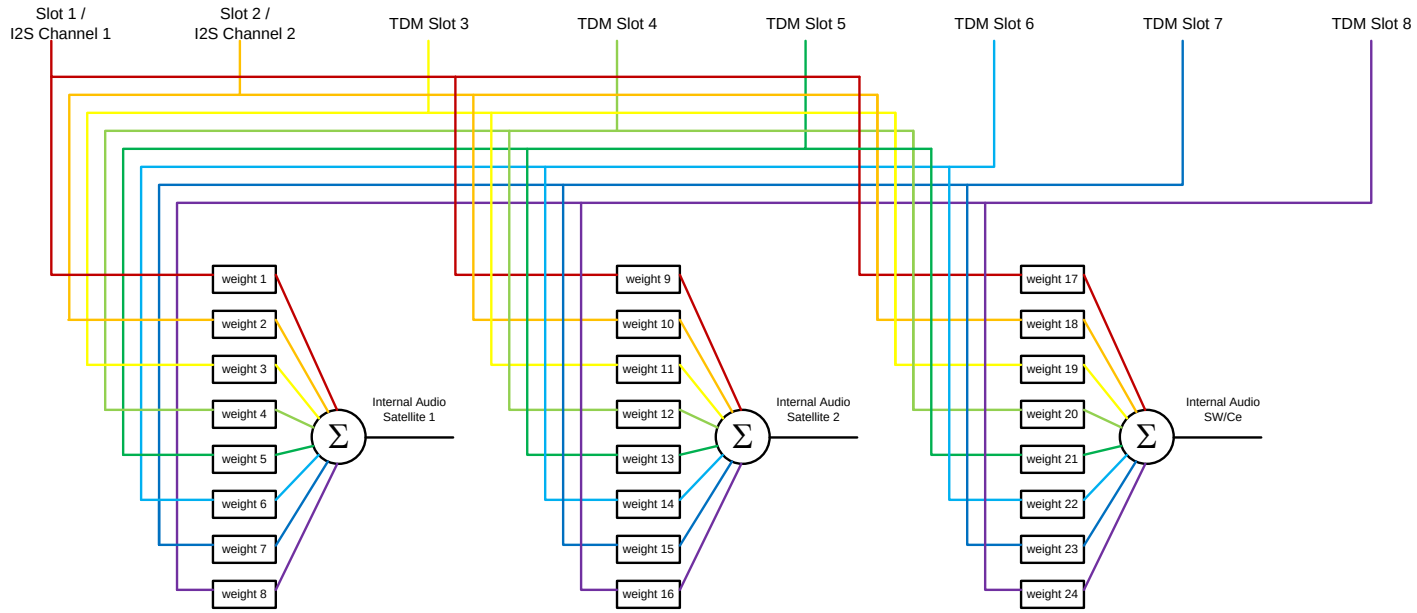


Figure 6-6 - Input Channel Scaling

6.4 Output Mixer

The Output Mixer assigns each of the output slots with one of the five audio streams from the core. There is no restriction on how the audio streams get assigned. A single audio stream may get assigned to zero, one, many, or all output slots/channels. QFPro provides easy assignment of these internal audio channels to output slots. Refer to the DOUT12_MAP registers for more detailed information.

TDM (dSDO1)	I2S/LJ/RJ	Register	Field
Slot 1	dSDO1 Left	DOUT12_MAP	slot1_src[2:0]
Slot 2	dSDO1 Right	DOUT12_MAP	slot2_src[2:0]
Slot 3	dSDO2 Left	DOUT34_MAP	slot3_src[2:0]
Slot 4	dSDO2 Right	DOUT34_MAP	slot4_src[2:0]
Slot 5	dSDO3 Left	DOUT56_MAP	slot5_src[2:0]
Slot 6	dSDO3 Right	DOUT56_MAP	slot5_src[2:0]
Slot 7	Not Applicable	DOUT78_MAP	slot6_src[2:0]
Slot 8	Not Applicable	DOUT78_MAP	slot7_src[2:0]

Table 6-2 - Register FieldTo Output Channel Map

6.5 dSDOn Output Enable Logic

6.5.1 DIN_PT Control

At times it may be desirable to pass the data present at **dSDI** directly to the **dSDOn** outputs.

If the **din_pt** cfg bit in the CONTROL register is set, **dSDI** will pass asynchronously through to **dSDOn** (albeit delayed by a few nanoseconds).

This control bit overrides all other settings for **dSDOn** and should be set to 0 when either configuring the chip or processing data.

6.5.2 FILT_EN Control

While the chips memories are being written to, **filt_en** must be set to a zero. During this time, if din_pt=0, all dSDOn outputs will be tristated. To enable signal processing, set **filt_en** to a one. The dSDOn pins will be driven then (depending on the following sections).

6.5.3 Normal Operation

6.5.3.1 dSDO1

Once **din_pt**=0 and **filt_en**=1, dSDO1 will:

- Drive internally processed data OR
- Drive data passed from dSDI unchanged OR
- Be tristated

With din_pt=0 and filt_en=1, the dSDO1 will drive out everyplace where there should be valid data coming from QF3DFX based on the selected protocols.

In the protocol sequence where there is no valid data to be driven:

- If pass_thru=0, the output will tristate. The pin can be driven weakly low or high, if desired, through the IO_dSDO1 config register.
- If pass_thru=1, the input will pass through to the output, incurring a few nanoseconds of delay..

6.5.3.2 dSDO2 and dSDO3

Unlike dSDO1, once din_pt=0 and filt_en=1, dSDO2 and dSDO3 will always be driven with either internally processed data (during times when valid data is expected within the frame) or zero's (during the time within a frame where no valid data is expected).

7 CONFIGURATION REGISTERS

7.1 Register Summary

Addr	Name	Description
00h	TEST_RW	Software Test; Reads & Writes
01h	CHIP_ID	Chip ID Number
02h	VERSION	Chip Version Number
03h	CONTROL	Mode Control
04h	DCONFIG	Data Format Control
05h	HFRAME_SIZE	Half Frame Size
06h	OFFSET1	Data Offset to Channel / Slot 1
07h	OFFSET2	Data Offset to Channel / Slot 2
08h	OFFSET3	Data Offset to Slot 3
09h	OFFSET4	Data Offset to Slot 4
0Ah	OFFSET5	Data Offset to Slot 5
0Bh	OFFSET6	Data Offset to Slot 6
0Ch	OFFSET7	Data Offset to Slot 7
0Dh	OFFSET8	Data Offset to Slot 8
13h	DOUT12_MAP	Output Channel/Slot Assignment 1,2
14h	DOUT34_MAP	Output Channel/Slot Assignment 3,4
15h	DOUT56_MAP	Output Channel/Slot Assignment 5,6
16h	DOUT78_MAP	Output Channel/Slot Assignment 7,8
17h	AGCS_THR_HI	Satellite AGC High Threshold
18h	AGCS_THR_LO	Satellite AGC Low Threshold
19h	AGCS_THR_NO	Satellite AGC Noise Threshold
1Ah	AGCS_ATTACK	Satellite AGC Attack Rate
1Ch	AGCS_RELEASE	Satellite AGC Release Rate
1Eh	AGCS_ALPHA	Satellite AGC Alpha
1Fh	AGCM_THR_HI	Mono AGC High Threshold
20h	AGCM_THR_LO	Mono AGC Low Threshold
21h	AGCM_THR_NO	Mono AGC Noise Threshold
22h	AGCM_ATTACK	Mono AGC Attack Rate
24h	AGCM_RELEASE	Mono AGC Release Rate
26h	AGCM_ALPHA	Mono AGC Alpha
28h	GEQ_P1_F1_GAIN	GEQ Profile 1 Filter 1 Gain
29h	GEQ_P1_F2_GAIN	GEQ Profile 1 Filter 2 Gain
2Ah	GEQ_P1_F3_GAIN	GEQ Profile 1 Filter 3 Gain

Addr	Name	Description
2Bh	GEQ_P1_F4_GAIN	GEQ Profile 1 Filter 4 Gain
2Ch	GEQ_P1_F5_GAIN	GEQ Profile 1 Filter 5 Gain
2Dh	GEQ_P2_F1_GAIN	GEQ Profile 2 Filter 1 Gain
2Eh	GEQ_P2_F2_GAIN	GEQ Profile 2 Filter 2 Gain
2Fh	GEQ_P2_F3_GAIN	GEQ Profile 2 Filter 3 Gain
30h	GEQ_P2_F4_GAIN	GEQ Profile 2 Filter 4 Gain
31h	GEQ_P2_F5_GAIN	GEQ Profile 2 Filter 5 Gain
32h	GEQ_P3_F1_GAIN	GEQ Profile 3 Filter 1 Gain
33h	GEQ_P3_F2_GAIN	GEQ Profile 3 Filter 2 Gain
34h	GEQ_P3_F3_GAIN	GEQ Profile 3 Filter 3 Gain
35h	GEQ_P3_F4_GAIN	GEQ Profile 3 Filter 4 Gain
36h	GEQ_P3_F5_GAIN	GEQ Profile 3 Filter 5 Gain
37h	GEQ_P4_F1_GAIN	GEQ Profile 4 Filter 1 Gain
38h	GEQ_P4_F2_GAIN	GEQ Profile 4 Filter 2 Gain
39h	GEQ_P4_F3_GAIN	GEQ Profile 4 Filter 3 Gain
3Ah	GEQ_P4_F4_GAIN	GEQ Profile 4 Filter 4 Gain
3Bh	GEQ_P4_F5_GAIN	GEQ Profile 4 Filter 5 Gain
3Ch	GEQ_P5_F1_GAIN	GEQ Profile 5 Filter 1 Gain
3Dh	GEQ_P5_F2_GAIN	GEQ Profile 5 Filter 2 Gain
3Eh	GEQ_P5_F3_GAIN	GEQ Profile 5 Filter 3 Gain
3Fh	GEQ_P5_F4_GAIN	GEQ Profile 5 Filter 4 Gain
40h	GEQ_P5_F5_GAIN	GEQ Profile 5 Filter 5 Gain
41h	GEQ_P6_F1_GAIN	GEQ Profile 6 Filter 1 Gain
42h	GEQ_P6_F2_GAIN	GEQ Profile 6 Filter 2 Gain
43h	GEQ_P6_F3_GAIN	GEQ Profile 6 Filter 3 Gain
44h	GEQ_P6_F4_GAIN	GEQ Profile 6 Filter 4 Gain
45h	GEQ_P6_F5_GAIN	GEQ Profile 6 Filter 5 Gain
46h	GEQ_P7_F1_GAIN	GEQ Profile 7 Filter 1 Gain
47h	GEQ_P7_F2_GAIN	GEQ Profile 7 Filter 2 Gain
48h	GEQ_P7_F3_GAIN	GEQ Profile 7 Filter 3 Gain
49h	GEQ_P7_F4_GAIN	GEQ Profile 7 Filter 4 Gain
4Ah	GEQ_P7_F5_GAIN	GEQ Profile 7 Filter 5 Gain
4Bh	GEQ_P8_F1_GAIN	GEQ Profile 8 Filter 1 Gain

Addr	Name	Description
4Ch	GEQ_P8_F2_GAIN	GEQ Profile 8 Filter 2 Gain
4Dh	GEQ_P8_F3_GAIN	GEQ Profile 8 Filter 3 Gain
4Eh	GEQ_P8_F4_GAIN	GEQ Profile 8 Filter 4 Gain
4Fh	GEQ_P8_F5_GAIN	GEQ Profile 8 Filter 5 Gain
50h	DYB_THR_HI	Dynamic Bass High Threshold
51h	DYB_THR_NO	Dynamic Bass Noise Threshold
52h	DYB_MAX_GAIN	Dynamic Bass Maximum Gain
53h	DYB_TRACK	Dynamic Bass Tracking Rate
54h	DYT_THR_HI	Dynamic Treble High Threshold
55h	DYT_THR_NO	Dynamic Treble Noise Threshold
56h	DYT_MAX_GAIN	Dynamic Treble Maximum Gain
57h	DYT_TRACK	Dynamic Treble Tracking Rate
58h	SPI_TO_I2C	SPI to 2C Status
59h	I2C_RDATA	I2C Read Data
5Ah	BOOT_STATUS	I2C Boot Status
5Bh	PRO_VOL_HADDR	Profile Volume High Address
5Ch	PRO_VOL_LADDR	Profile Volume Low Address
5Dh	PRO_CTRL	Master Profile Control
5Eh	CUR_VOL	Master Profile Volume
5Fh	MAX_VOL	Maximum Master Volume
60h	VSLEW	Profile Volume Slew Rate
62h	BTNCTRL	Button and Tone Control

Addr	Name	Description
63h	AMP_DROP	Amplifier Protection
64h	TONE_GEN	Tone Control
89h	IO_DSCK	Data Clock Pin Control, dSCK
8Ah	IO_DCS	Data Chip Select Pin Control, dCS
8Bh	IO_DSDI	I2S/TDM Data In Pin Control, dSDI
8Ch	IO_CS_N	Configuration Chip Select Pin Control, cCSn
8Dh	IO_SCLK	Configuration Clock Pin Control, cSCK
8Eh	IO_SDI	SPI In Pin Control, cSDI
8Fh	IO_SAD1	I2C Address 1 Pin Control, cSAD1
90h	IO_SAD2	I2C Address 2 Pin Control, cSAD2
91h	IO_VUP & VDN	Volume Up Pin Control, VUP & VDN
92h	NA1	Not used
93h	IO_PRO	Profile Pin Control, PROF
94h	IO_AMP	Amp Pin Control, AMP
95h	IO_MUTE	Mute Pin Control, MUTE
96h	IO_SCL	I2C SCL Pin Control, cSCL
97h	IO_SDA	I2C SDA Pin Control, cSDA
98h	IO_SDO	Configuration Output Pin Control, SDO
99h	IO_DSDO1	Data Output 1 Pin Control, dSDO1
9Ah	IO_DSDO2	Data Output 2 Pin Control, dSDO2
9Bh	IO_DSDO3	Data Output 3 Pin Control, dSDO3

Table 7-1 - Register Summary

7.2 Register Definitions

Access the configuration registers using the SPI or I2C protocol as described in Section 4

WARNING Do not write to any addresses not shown here.

00h TEST_RW - Software Test; Reads and Writes

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW
Bits	TEST							
TEST	Provided as a developer debug read and write test register.							

01h CHIP_ID - Chip ID Number

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	1	1	0	1	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Bits	**id**							
id	Read-only byte containing the identification number for the QF3DFX device, D0h.							

02h VERSION - Chip Version Number

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	0	0	0	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Bits	**ver**							
ver	Read-only byte containing the version number for the QF3DFX device, 01h.							

03h CONTROL - Mode Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RW	RW
Bits	R	R	R	R	R	R	**din_pt**	**filt_en**
din_pt	Data In Pass Through (**din_pt**) : Puts the QF3DFX in Bypass mode 0 = Normal operation - dSDOn pins output the internal signal path data. 1 = Data pass through (asynchronous flow-through) - dSDOn pins output the data on the dSDI pin							
filt_en	Filter Enable (**filt_en**) : Enable the signal processing blocks and data path 0 = Configuration mode, signal processing disabled, access unlimited – access to all memory spaces. In this mode the dSDOn outputs are tristated. 1 = Filter mode, signal processing enabled, access limited to configuration and volume space only							

04h DCONFIG - Data Format Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	1	1	0	0	0	0	1
Access	RO	RW	RW	RW	RW	RW	RW	RW
Bits	R	**dsize**	**pass_thru**	**mode**		**format**	**dcs_pol**	**dsck_pol**

dsize	Sets the data width 0 = 16-bit 1 = 24-bit
pass_thru	In TDM Mode, determines how dSDO1 behaves during bit-clocks in a frame when it is not driving valid 16-bit or 24-bit data. This field is ignored in I2S, Left Justified, and Right Justified modes. 0 = dSDO1 tristates when not driving valid data. 1 = dSDO1 drives all of the time. Incoming dSDI passes asynchronously through the chip to dSDO1 when the chip is not driving valid 16-bit or 24-bit data.
mode	Selects the data input mode. 00 = I2S 01 = Left Justified 10 = Right Justified 11 = TDM (Time Division Multiplexed)
format	Selects the data format of the incoming data. This field is ignored in I2S, Left Justified, and Right Justified modes. 0 = Incoming data format is 2's complement. 1 = Incoming data format is offset binary.
dcs_pol	Selects the edge of dCS that defines the start of a frame (one complete sample period) of data. This field is ignored in I2S, Left Justified, and Right Justified modes. 0 = The start of a frame is based from the falling edge of dCS_POL. 1 = The start of a frame is based from the rising edge of dCS_POL..
dsck_pol	The clock edge of dSCK on which the dSDI data is captured. dSDO is output on the opposite edge. 0 = dSDI data is captured on the falling edge of dSCK. 1 = dSDI data is captured on the rising edge of dSCK.

05h HFRAME_SIZE - Half Frame Size

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	1	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**hfs**							

hfs	This field must be set to ½ the number of bit clocks in a sample frame. This applies to all four transfer protocols (I2S, LJ, RJ, and TDM). For example, in a system where the I2S frame contains two 32-bit slots, this register must be programmed to 64 * 1/2 = 32 decimal (20 hex). Frames sizes above 510 are not supported, as this would require a Half Frame Size greater than 255 decimal.

06h – 0Dh OFFSET1-8 - Data Offset to Channel / Slot

Address	POR							
Channel, Slot	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h, 1	0	0	0	0	0	0	0	1
07h, 2	0	0	1	0	0	0	0	1
08h, 3	0	1	0	0	0	0	0	1
09h, 4	0	1	1	0	0	0	0	1
0Ah, 5	1	0	0	0	0	0	0	1
0Bh, 6	1	0	1	0	0	0	0	1
0Ch, 7	1	1	0	0	0	0	0	1
0Dh, 8	1	1	1	0	0	0	0	1
Access	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**doffset**							
doffset	In TDM Mode, determines the offset to the start of data samples within a frame when. The first bit sampled after the active dCS edge has an offset of 0. Normally, adjacent slot's data offsets will differ by the slot size (e.g. with a slot size of 32. Up to eight slot offsets can be programmed. POR values are appropriate for TDM where the Most Significant Bit is offset by one bit clock from the start of each slot within the frame, with a slot size of 32 bit-clocks. These fields are ignored when the MODE bits are not set to TDM. These fields are ignored in I2S, Left Justified, and Right Justified modes.								

13h – 16h DOUT12_MAP, DOUT34_MAP, DOUT56_MAP, DOUT78_MAP - Output Channel / Slot Assignments

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
13h, POR	0	0	0	1	1	0	0	0
14h – 16h, POR	0	0	1	1	1	1	1	1
Access	RO	RO	RW	RW	RW	RW	RW	RW
13h	R	R	**slot2_src**				**slot1_src**	
14h	R	R	**slot4_src**				**slot3_src**	
15h	R	R	**slot6_src**				**slot5_src**	
16h	R	R	**slot8_src**				**slot7_src**	
slot1_src **slot2_src** **slot3_src** **slot4_src** **slot5_src** **slot6_src** **slot7_src** **slot8_src**	Assigns an internal channel to an output slot 000 = Satellite channel 1 or Satellite channel 1 low 001 = Mono channel 010 = Satellite channel 1 high 011 = Satellite channel 2 or satellite channel 2 low 100 = Not used 101 = Satellite channel 2 high 110 = No assignment (output slot is disabled) 111 = No assignment (output slot is disabled) In TDM Mode, if an output slot is disabled, the data on that slot is determined by the **pass_thru** field in the Data Format Control register.							

17h AGCS_THR_HI - Satellite AGC High Threshold

1Fh AGCM_THR_HI - Mono AGC High Threshold

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	0	0	0	0	0
Access	RO	RW	RW	RW	RW	RW	RW	RW
17h	R	**sat_thr_hi**						
1Fh	R	**mon_thr_hi**						
sat_thr_hi **mon_thr_hi**	AGC High threshold These represent an average amplitude level measured in dB down from Digital Full Scale (dBFS) according to the following formula. High Threshold in dBFS = -2 * **sat_thr_hi** (or **mon_thr_hi**) For example, if **sat_thr_hi** = 13 decimal, the Satellite AGC High Threshold is -2*13 = -26 dBFS Values of 73 and above (equating to -146 dBFS and lower) equate to exactly zero amplitude (-dBFS). There is lower precision at very low dBFS values (below -128 dBFS). Unpredictable results may occur if the **sat_thr_hi** value is less than the Satellite AGC Low Threshold (**sat_thr_lo**) or the Satellite AGC Noise Threshold (**sat_thr_no**). The same is true for **mon_thr_hi** with **mon_thr_lo** and **mon_thr_no**.							

18h AGCS_THR_LO - Satellite AGC Low Threshold

20h AGCM_THR_LO - Mono AGC Low Threshold

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	0	0	0	0	0
Access	RO	RW	RW	RW	RW	RW	RW	RW
18h	R	**sat_thr_lo**						
20h	R	**mon_thr_lo**						
sat_thr_lo **mon_thr_lo**	AGC Low Threshold These represent an average amplitude level measured in dB down from Digital Full Scale (dBFS) according to the following formula. Low Threshold in dBFS = -2 * **sat_thr_lo** (or **mon_thr_lo**) For example, if **sat_thr_lo** = 24 decimal, the low threshold is -2*24 = -48 dBFS Values for this register of 73 and above (equating to -146 dBFS and lower) equate to exactly zero amplitude (-dBFS). There is lower precision at very low dBFS values (below -128 dBFS). Unpredictable results may occur if the Satellite AGC Low Threshold (**sat_thr_lo**) is greater than the Satellite AGC High Threshold (**sat_thr_hi**) or less than the Satellite AGC Noise Threshold (**sat_thr_no**). The same is true for **mon_thr_lo** with **mon_thr_hi** and **mon_thr_no**.							

19h AGCS_THR_NO - Satellite AGC Noise Threshold

21h AGCM_THR_NO - Mono AGC Noise Threshold

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	0	0	0	0	0
Access	RO	RW	RW	RW	RW	RW	RW	RW
19h	R	**sat_thr_no**						
21h	R	**mon_thr_no**						
sat_thr_no **mon_thr_no**	AGC noise threshold These represent an average amplitude level measured in dB down from Digital Full Scale (dBFS) according to the following formula. Noise Threshold in dBFS = -2 * **sat_thr_no** (or **mon_thr_no**) For example, if **sat_thr_no** = 40 decimal, the low threshold is -2*40 = -80 dBFS Values for this register of 73 and above (equating to -146 dBFS and lower) equate to exactly zero amplitude (-dBFS). There is lower precision at very low dBFS values (below -128 dBFS). Unpredictable results may occur if the Satellite AGC Noise Threshold (**sat_thr_no**) is greater than the Satellite AGC High Threshold (**sat_thr_hi**) or the Satellite AGC Low Threshold (**sat_thr_lo**). The same is true for **mon_thr_no** with **mon_thr_hi** and **mon_thr_lo**.							

1Ah/1Bh AGCS_ATTACK - Satellite AGC Attack Rate

1Fh/20h AGCM_ATTACK - Mono AGC Attack Rate

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
POR	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW
1Ah	**satk[7:0]**							
1Bh	**satk[15:8]**							
1Fh	**matk[7:0]**							
20h	**matk[15:8]**							
satk **matk**	AGC Attack Rate These each represent a positive fractional value ranging linearly from 0.0 to slightly less than 1.0. It helps control the rate at which the AGC gain is reduced when the average Satellite or Mono Channel signal amplitude is above the corresponding AGC High Threshold (either Satellite or Mono Channel). Higher values mean the current AGC gain will be reduced more quickly, which will in turn lower the average AGC signal amplitude. The Satellite Channel AGC's operate independently, but receive the same settings. The Mono AGC is completely independent of the Satellite AGC's. Refer to the AGC Section for more information.							

1Ch/1Dh AGCS_RELEASE - Satellite AGC Release Rate

21h/22h AGCM_RELEASE - Mono AGC Release Rate

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
POR	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW
1Ch	**srel[7:0]**							
1Dh	**srel[15:8]**							
21h	**mrel[7:0]**							
22h	**mrel[15:8]**							
srel **mrel**	AGC Attack Rate These each represents a positive fractional value ranging linearly from 0.0 to slightly less than 1.0. It helps control the rate at which the AGC gain is increased when the average Satellite or Mono Channel signal amplitude is below the corresponding AGC Low Threshold (either Satellite or Mono Channel) AND above the corresponding AGC noise Threshold (either Satellite or Mono Channel). Higher values mean the current AGC gain will be increased more quickly, which will in turn raise the average AGC signal amplitude. The Satellite Channel AGC's operate independently, but receive the same settings. The Mono AGC is completely independent of the Satellite AGC's. Refer to the AGC Section for more information.							

1Eh AGCS_ALPHA - Satellite AGC Alpha

26h AGCM_ALPHA - Mono AGC Alpha

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RW	RW	RW	RW	RW
1Eh	R	R	R	**salpha**				
26h	R	R	R	**malpha**				
salpha **malpha**	AGC alpha (feed forward term) value These each represent a positive fractional value ranging 0.01 to 0.5 in 31 logarithmically spaced steps. This fractional value becomes the alpha term in a 1st order IIR that measures the average AGC amplitude (each Satellite channel and the Mono Channel are independent of each other). Higher values mean the IIR will respond more quickly to average signal level changes. Lower values mean the IIR will respond more slowly to average signal level changes. **salpha** applies to each Satellite Channel. **malpha** applies only to the Mono Channel.							

28h – 4Fh GEQ_Pm_Fn_GAIN - GEQ Profile Filter Gains

GEQ Register Addresses		Profile (m)							
		1	2	3	4	5	6	7	8
Filter (n)	1	28h	2Dh	32h	37h	3Ch	41h	46h	4Bh
	2	29h	2Eh	33h	38h	3Dh	42h	47h	4Ch
	3	2Ah	2Fh	34h	39h	3Eh	43h	48h	4Dh
	4	2Bh	30h	35h	3Ah	3Fh	44h	49h	4Eh
	5	2Ch	31h	36h	3Bh	40h	45h	4Ah	4Fh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RW	RW	RW	RW	RW
Bits	R	R	R	**geqgain**				
geqgain	Gain value; 0 to -31dB in 1dB steps 0 = 0dB 1 = -1dB … 31 = -31 dB Each of the eight profiles above (designated by the PN columns) contains five filters (designated by the Filter rows), each of which can have a unique gain. This is a total of 40 filter gains in all.							

50h DYB_THR_HI - Dynamic Bass High Threshold

54h DYT_THR_HI - Dynamic Treble High Threshold

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	1	0	1	0	0
Access	RO	RO	RW	RW	RW	RW	RW	RW
50h	R	R	**dyb_thr_hi**					
54h	R	R	**dyt_thr_hi**					
dyb_thr_hi **dyt_thr_hi**	Dynamic Bass and Dynamic Treble High Thresholds For Dynamic Bass (**dyb_thr_hi**), this represents an average amplitude level measured in dB down from Digital Full Scale (dBFS). When the low-passed average amplitude of the incoming signal is higher than this threshold, no gain is applied to the signal. When the low-passed average amplitude of the incoming signal is lower than this threshold, a gain is applied to the low frequency component. Exactly how much gain is applied depends on other parameters. 0 = 0 dB 1 = -1 dB etc. For example, if **dyb_thr_hi** = 13 decimal, the High Threshold is = -13 dBFS For Dynamic Treble (**dyt_thr_hi**), the operation is exactly the same, except the amplitude being measured, and the gain applied to it, is the high-pass filtered amplitude content, not the low-pass content.							

51h DYB_THR_NO - Dynamic Bass Noise Threshold

55h DYT_THR_NO - Dynamic Treble Noise Threshold

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	1	1	1	0	0
Access	RO	RO	RW	RW	RW	RW	RW	RW
51h	R	R	**dyb_thr_no**					
55h	R	R	**dyt_thr_no**					
dyb_thr_no **dyt_thr_no**	Dynamic Bass and Dynamic Treble Noise Threshold For Dynamic Bass (**dyb_thr_no**), this represents an average amplitude level measured in dB down from Digital Full Scale (dBFS) according to the following equation: Noise Threshold in dBFS = -(**dyb_thr_no** + 32) For example, when **dyb_thr_no** = 19 decimal, the Noise Threshold is –(19+32) = -51 dBFS The output of the 1st Exp. Averager in the Dynamic Bass Block is compared against this value. When the output is lower than **dyb_thr_no**, the 2nd Exp. Averaging IIR is not updated. When the output is higher than **dyb_thr_no**, the 2nd Exp. Averaging IIR is updated. The intent is that when the input consists of noise or very low level signals (such as during quiet times in music), the Dynamic Bass block won't continue updating itself, potentially adding significant gain to the Low Passed portion of the signal. For Dynamic Treble (**dyt_thr_no**), the operation is exactly the same, except the amplitude being measured, and the gain applied to it, is the high-pass filtered amplitude content, not the low-pass content.							

52h DYB_MAX_GAIN - Dynamic Bass Maximum Gain

56h DYT_MAX_GAIN - Dynamic Treble Maximum Gain

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	0	1	1	0	0
Access	RO	RO	RO	RO	RW	RW	RW	RW
52h	R	R	R	R	**dyb_maxgain**			
56h	R	R	R	R	**dyt_maxgain**			
dyb_maxgain **dyt_maxgain**	Dynamic Bass and Dynamic Treble Maximum Gain For Dynamic Bass (**dyb_max_gain**), this represents the maximum gain that will be applied by the Dynamic Bass Block to the low pass filtered portion of the signal. For example, when **dyb_maxgain** = 9 decimal, the maximum gain to be applied is 9dB. For Dynamic Treble (**dyt_maxgain**), the operation is exactly the same, except the maximum gain limit is applied to high-pass filtered content, not low-pass filtered content.							

54h DYB_TRACK - Dynamic Bass Tracking Rate

57h DYT_TRACK - Dynamic Treble Tracking Rate

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	0	0	0	1	1
Access	RO	RO	RO	RO	RO	RO	RW	RW
54h	R	R	R	R	R	R	**dyb_trk**	
54h	R	R	R	R	R	R	**dyt_trk**	
dyb_trk **dyt_trk**	Dynamic Bass and Dynamic Treble Tracking Rates For Dynamic Bass (**dyb_trk**), this represents the rate at which the gain applied to the Low Pass filtered signal will be increased as the average signal level drops below the Dynamic Bass High Threshold level. 00 = For every dB drop, 1.00 dB of gain will be applied to the low-pass filtered signal content. 01 = For every dB drop, 0.75 dB of gain will be applied to the low-pass filtered signal content. 10 = For every dB drop, 0.50 dB of gain will be applied to the low-pass filtered signal content. 11 = For every dB drop, 0.25 dB of gain will be applied to the low-pass filtered signal content. For Dynamic Treble (**dyt_trk**), the operation is exactly the same, except the tracking rate is applied to high-pass filtered content, not low-pass filtered content.							

58h SPI_TO_I2C - SPI to I2C Status

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	1	0	0	0	0
Access	RO	RO	RO	RW	RO	RO	RO	RO
Bits	R	R	R	**eesize**	**rdvalid**	**pdone**	**tabort**	**wdone**
wdone	SPI to I2C Write Done Flag This bit goes low when a SPI to I2C write is initiated by an external SPI master. It returns high when the write is complete on the I2C bus. It works with the **tabort** flag below. The two of them will never be high together. 0 = The SPI to I2C write is pending on the I2C bus 1 = The SPI to I2C write completed successfully.							
tabort	SPI to I2C Target Abort Flag This bit goes low when a SPI to I2C write or read is initiated by an external SPI master. It returns high if the I2C operation ends in a Target Abort. It works with the **wdone** flag above and the **rdvalid** flag below. **tabort** and **wdone** will never be high together. **tabort** and **rdvalid** will never be high together. 0 = The SPI to I2C write is pending on the I2C bus 1 = The SPI to I2C write completed successfully.							
pdone	EEPROM Page Done Flag This bit is set whenever a write is done to the last byte in a page, and the whole page must then be written in the EEPROM. This is only for status. An external SPI master does not need to react differently when this bit is set vs. when it is clear. 0 = The last byte written was not at the end of a page in the EEPROM 1 = The last byte written to the EEPROM was at the end of a page.							
rdvalid	Read Data Valid Flag This bit indicates when valid read data is available after a command is sent to perform a SPI to I2C read. It goes low when the SPI to I2C command is received and stays low until valid data has been received. 0 = Valid Read Data is not yet available 1 = Valid Read Data is available and can be read at I2C_RDATA register.							
eesize	**eesize** indicates which kind if EEPROM will be accessed by subsequent SIB to I2C EEPROM accesses: 0 = 8 bit EEPROM (no longer supported) 1 = 16 bit EEPROM							

59h I2C_RDATA - I2C Read Data

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Bits	**i2c_rdata**							
i2c_rdata	**i2c_rdata** is the data returned from the I2C during a SPI to I2C read command. It is valid after the **rdvalid** bit has been set in the SPI_TO_I2C register.							

5Ah BOOT_STATUS - Boot Status

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Bits	R	R	**mdone**	**dnf**	**chksum**	**siginv**	**baabort**	**bootok**
bootok	Boot OK Flag Indicates if the Boot Sequence completed successfully or not. This means that either there was no EEPROM found or that there was an EEPROM found and was booted from successfully. 0 = Boot Failed 1 = Boot OK							
babort	Boot Target Abort Flat Indicates if a target abort occurred during the boot sequence. This would occur if no 8-bit device was found, but a 16-bit device was found, since when the 8-bit device access was attempted, a target abort would occur. 0 = No Target abort occurred 1 = A Target abort occurred sometime during the boot process.							
siginv	Signature Invalid Flag Indicates if an invalid signature was found or not. An invalid signature is when the first three bytes of the EEPROM header are not ascii 'Q', 'F', and 'T' respectively. 0 = Signature Valid (or no EEPROM found) 1 = Signature invalid							
chksum	CHKSUM Error Flag Indicates if a checksum error was found or not. An checksum error is when the checksum of the first 16 bytes of the header doesn't sum to 0x00 (upper bits ignored) 0 = Valid Checksum found or no EEPROM found) 1 = Checksum invalid							
dnf	Device Not Found Flag Indicates if neither an 8-bit nor a 16-bit EEPROM was found at the address determined by the SADx pins. 0 = An 8-bit or 16-bit EEPROM was found 1 = Device not found							
mdone	Boot Master Done Flag Indicates if the I2C Master is done with the boot sequence or not. Once this bit is set, the other bits in this register may be examined to determine how successful the boot sequence was. 0 = Master is not yet done 1 = Master done							

5Bh PRO_VOL_HADDR - Profile Volume High Address

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**pvhaddr**							
pvhaddr	Profile / Volume EEPROM Address High Byte When the VUP, VDN, or PROF pins cause the selected volume or profile to change, the updated profile and volume values are written to an EEPROM at the address set by **pvhaddr** prepended to **pvladdr**.							

5Ch PRO_VOL_LADDR - Profile Volume Low Address

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW
Bits	**pvladdr**							
pvladdr	Profile / Volume EEPROM Address Low Byte When the VUP, VDN, or PROF pins cause the selected volume or profile to change, the updated profile and volume values are written to an EEPROM at the address set by **pvhaddr** prepended to **pvladdr**.							

5Dh PRO_CTRL – Master Profile Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	1	1	1	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW
Bits	R	R	**maxprof**			**curprof**		
curprof	**curprof** is the currently selected profile, of which there are eight, indexed as 0 to 7. This value can be modified by the PROF pin or by an I2C or SPI master writing into the register. If this register is modified due to the PROF pin, and a valid EEPROM exists in the I2C address space, the new register value will be written to the EEPROM at the location indicated by the PRO_VOL_HADDR and PRO_VOL_LADDR registers.							
maxprof	**maxprof** is the highest profile that will be selected when using the PROF pin to cycle through the profiles. When using the PROF pin, no I2C or SPI master should program **maxprof** to be less than **curprof**. This register is not referenced if the PROF pin is not used.							

5Eh CUR_VOL - Master Volume Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	1	1	0	0	0	1	1
Access	RW	RW	RW	RW	RW	RW	RW	RW
Bits	R	**curvol**						
curvol	**curvol** is the current index into the Volume Table. This value can be modified by the VUP/VDN pins or by an I2C or SPI master writing into the register. If this register is modified due to VUP or VDN, and a valid EEPROM exists in the I2C address space, the new value will be written to the EEPROM at the location indicated by the PRO_VOL_HADDR and PRO_VOL_LADDR registers. Valid values are 0 decimal to 99 decimal. An external master writing values above 99 decimal will result in undefined behavior.							

5Fh MAX_VOL - Maximum Master Volume

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	1	1	0	0	0	1	1
Access	RO	RW	RW	RW	RW	RW	RW	RW
Bits	R	**maxvol**						
maxvol	**maxvol** is the highest index that will be selected when traversing the Volume Table using the VUP and VDN pins. Valid values are 0 decimal to 99 decimal. Assigning this register a value above 99 decimal and then using the VUP or VDN pins will result in undefined behavior. When using the VUP/VDN pins, no I2C or SPI master should program **maxvol** to be less than **curvol**. This register is not referenced if the Current Master Volume register is updated solely by an I2C or SPI master.							

60h VSLEW - Volume Slew Rate

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	RW	RW	RW	RW
Field Name	R	R	R	R	**slew**			
slew	Slew Rate for Master Volume, GEQ, MUTE, and Amp Protection circuitry Whenever the volume changes due to an adjustment in the master volume, GEQ, MUTE or amplifier protection circuitry, the actual gain applied to the circuitry is a slewed gain. The slew rate is sample rate dependent. At 48 kHz the following table is true. Halving the sample rate will double the slew rate, etc. 0 = 48 dB/ms 1 = 24 dB/ms 2 = 12 dB/ms 3 = 6 dB/ms 4 = 3 dB/ms 5 = 1.5 dB/ms 6 = 0.75 dB/ms 7 = 0.375 dB/ms 8 = 0.188 dB/ms 9 = 94 dB/sec 10 = 47 dB/sec 11 = 23 dB/sec 12, 13, 14 = N/A Do Not Use 15 = Instantaneous							

62h BTNCTRL – Volume Pins (usually tied to Buttons) and Tone Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	0	0	0	0	0
Access	RO	RO	RW	RW	RW	RW	RW	RW
Bits	R	R	**ben**	**volsus**	**mute**	**vdn**	**vup**	**prof**

prof	0 = No tone is produced when the PROF pin is asserted low 1 = A tone is produced when the PROF pin is asserted low and BEN = 1
vup	Controls whether a tone is produced when the VDN pin is driven low. 0 = No tone is produced when the VUP pin is asserted low 1 = A tone is produced when a) the VUP pin is asserted low and b) **ben** = 1 and c) the CUR_VOL register is not equal to MAX_VOL
vdn	Controls whether a tone is produced when the VDN pin is driven low. 0 = No tone is produced when the VDN pin is asserted low 1 = A tone is produced when a) the VDN pin is asserted low and b) **ben** = 1 and the CUR_VOL register is not equal to 0
mute	Controls whether a tone is produced when the MUTE pin is driven low. 0 = No tone is produced when the MUTE pin is asserted low 1 = A tone is produced when the MUTE pin is asserted low and **ben** = 1 Note: A tone may only partially be heard because the muting function may be attenuating the signal during the time the tone is being played.
volsus	Controls whether a tone is repeatedly produced when the VUP or VDN pins are driven low and held. Holding either of these two pins low will cause the volume pointer to step repeated up or down the volume table. 0 = No tone is produced under the above conditions 1 = A brief tone is repeatedly produced when the VUP or VDN pins are driven low and held for more than two seconds, and **ben** = 1
ben	Enables the four volume related pins (VUP, VDN, MUTE, PROF) 0 = All pins disabled (asserting any of them low will have no effect) 1 = all pins enabled

63h AMP_DROP - Amplifier Protection

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	0	0	0	1	1
Access	RO	RO	RO	RW	RW	RW	RW	RW
Bits	R	R	R	**amp_drop**				

amp_drop	This represents how many dB the Master Gain will be reduced by when the AMP pin is asserted. Any amplitude change will be slewed according to the Profile Volume Slew amount, and thus be somewhat gradual. 0 = 0 dB drop 1 = 1 dB drop . . . The maximum drop is 31 dB.

64h TONE_GEN - Tone Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RW	RW
Bits	R	R	R	R	R	R	**tone2en**	**tone1en**
tone1en	Tone 1 Generation controlled by an external microprocessor 0 = Tone 1 Disabled 1 = Tone 1 Enabled							
tone2en	Tone 2 Generation controlled by an external microprocessor 0 = Tone 2 Disabled 1 = Tone 2 Enabled							

87h – 95h IO_XXX - Input Pins Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Access	RO	RO	RO	RO	RO	RW	RW	RW
Bits	R	R	R	R	R	**pu_en**	**pd_en**	**smt_en**
89h, dSCK	0	0	0	0	0	0	0	1
8Ah, dCS	0	0	0	0	0	0	0	1
8Bh, dSDI	0	0	0	0	0	0	0	1
8Ch, cCSn	0	0	0	0	0	1	0	1
8Dh, cSCK	0	0	0	0	0	0	1	1
8Eh, cSDI	0	0	0	0	0	0	1	1
8Fh, cSAD1	0	0	0	0	0	0	1	0
90H, cSAD2	0	0	0	0	0	0	1	0
91h, VUP & VDN*	0	0	0	0	0	1	0	1
93h, PROF	0	0	0	0	0	1	0	1
94h, AMP	0	0	0	0	0	0	1	1
95h, MUTE	0	0	0	0	0	1	0	1
pu_en	Enables the pull up resistor on the pin. 0 = No pull up resistor on input. 1 = 75K Ohm pull up resistor on input							
pd_en	Enables the pull down resistor on the pin. 0 = No pull down resistor on input. 1 = 75K Ohm pull down resistor on input.							
smt_en	Enables the Schmitt trigger input on the pin. 0 = Normal input. 1 = Schmitt trigger input.							

* The config bits in address 0x91 control both the VUP and the VDN pins. The config bits in address 0x92 exist as in address 0x91, but do not perform any function.

96h – 97h IO_XXX – Bidirectional Pins Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Access	RO	RW	RW	RW	RW	RW	RW	RW
Bits	R	**drive**			**sr**	**pu_en**	**pd_en**	**spr**
96h, cSCL	0	1	0	0	0	1	0	0
97h, cSDA	0	1	0	0	0	1	0	0

drive	Determines the drive strength of the output driver. VDDIO 3.3V / 2.5 V / 1.8 V 0 = 2 mA / 1.1 mA / 0.7 mA 1 = 4 mA / 2.2 mA / 1.4 mA 2 = 6 mA / 3.3 mA / 2.1 mA 3 = 8 mA / 4.4 mA / 2.8 mA 4 = 10 mA / 5.5 mA / 3.5 mA (POR) 5 = 12 mA / 6.6 mA / 4.2 mA 6 = 14 mA / 7.7 mA / 4.9 mA 7 = 16 mA / 8.8 mA / 5.6 mA
sr	Controls the Slew Rate of the output driver. 0 = Fast 1 = Slow
pu_en	Enables the pull up resistor on the pin. 0 = No pull up resistor on input. 1 = 75K Ohm pull up resistor on input
pd_en	Enables the pull down resistor on the pin. 0 = No pull down resistor on input. 1 = 75K Ohm pull down resistor on input.
spr	These are spare unused bits. Schmitt triggering is always enabled on cSCL and cSDA.

96h – 97h IO_XXX – Output Pins Control

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Access	RO	RO	RO	RO	RW	RW	RW	RW
Bits	R	R	R	R	**drive**			**sr**
98h, SDO	0	0	0	0	1	0	0	0
99h, dSDO1	0	0	0	0	1	0	0	0
9Ah, dSDO2	0	0	0	0	1	0	0	0
9Bh, dSDO3	0	0	0	0	1	0	0	0
drive	Determines the drive strength of the output driver. VDDIO 3.3V / 2.5 V / 1.8 V 0 = 2 mA / 1.1 mA / 0.7 mA 1 = 4 mA / 2.2 mA / 1.4 mA 2 = 6 mA / 3.3 mA / 2.1 mA 3 = 8 mA / 4.4 mA / 2.8 mA 4 = 10 mA / 5.5 mA / 3.5 mA (POR) 5 = 12 mA / 6.6 mA / 4.2 mA 6 = 14 mA / 7.7 mA / 4.9 mA 7 = 16 mA / 8.8 mA / 5.6 mA							
sr	Controls the Slew Rate of the output driver. 0 = Fast 1 = Slow							

8 ELECTRICAL SPECIFICATION

8.1 Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Parameter	Min	Max	Units
Storage Temperature	-40	150	ºC
Supply Voltage, V_{DD18} to GND	-0.3	2.16	V
Supply Voltage, V_{DD33} with respect to GND	-0.3	4.0	V
Digital Input Voltage with respect to GND	-0.3	4.0	V
Digital Input Voltage with respect to V_{DD33}		0.7	V
ESD Immunity (HBM, JESD22-A114-D Class 1C)		7.5	KV
ESD Immunity (HBM, AEC-Q100-002D)		6.75	KV

This integrated circuit can be damaged by ESD. Quickfilter Technologies recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

8.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage 1.8	V_{DD18}	1.62	1.8	1.98	V
Supply Voltage 3.3	V_{DD33}	3.0		3.6	V
Ambient Temperature	T_A	-40	25	85	ºC

Note: Quickfilter guarantees the performance of this device over specified ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling.

8.3 Typical Performance Characteristics

Default Conditions: T_A = 25 C, V_{DDCORE} = 1.8V,

IO Cell characteristics fall under one of three voltage levels appropriate to the V_{DD33} voltage:

3.3 Volt LVTTL for V_{DD33} = 3.3V +/- 10%

2.5 Volt CMOS for V_{DD33} = 2.5V +/- 10%

1.8 Volt CMOS for V_{DD33} = 1.8V +/- 10%

The QF3DFX will operate with any V_{DD33} voltage between 3.63 V and 1.62 V, as long as appropriate input and output levels/loading are observed.

8.3.1 DC Electrical Characteristics

3.3V TTL - Conditions: V_{DD33} = 3.3V +/- 10%

Symbol	Parameter (Condition)	Min	Typ	Max	Units	Note
V_{IL}	Low-level Input Voltage, V_{DD33} = 2.97V	-0.3		0.8	V	
V_{IH}	High-level Input Voltage, V_{DD33} = 3.63V	2.0		3.63	V	
V_T	Switching Threshold (Non-Schmitt triggered)		1.6		V	
V_{T-}	Switching Threshold (Schmitt triggered – negative edge)	0.8	1.25		V	
V_{T+}	Switching Threshold (Schmitt triggered – positive edge)		1.75	2.0	V	
R_{PU}	Pull Up Resistance	40	75	190	KOhm	
R_{PD}	Pull Down Resistance	40	75	190	KOhm	
V_{OL}	Low-level Output Voltage, V_{DD33} = 3.63V, I_{OL} = 2mA ~ 16mA			0.4	V	1
V_{OH}	High-level Output Voltage, V_{DD33} = 2.97V, I_{OH} = -2mA ~ -16mA	2.4			V	1

2.5V CMOS - Conditions: V_{DD33} = 2.5V +/- 10%

Symbol	Parameter (Condition)	Min	Typ	Max	Units	Note
V_{IL}	Low-level Input Voltage (V_{DD33} = 2.25V)	-0.3		0.25 * V_{DD33}	V	
V_{IH}	High-level Input Voltage (V_{DD33} = 2.75V)	0.63 * V_{DD33}		2.75	V	
V_T	Switching Threshold (Non-Schmitt triggered)		1.15		V	
V_{T-}	Switching Threshold (Schmitt triggered – negative edge)	0.25 * V_{DD33}	0.94		V	
V_{T+}	Switching Threshold (Schmitt triggered – positive edge)		1.4	0.63 * V_{DD33}	V	
R_{PU}	Pull Up Resistance	45	110	290	KOhm	
R_{PD}	Pull Down Resistance	45	115	290	KOhm	
V_{OL}	Low-level Output Voltage, V_{DD33} = 3.63V, I_{OL} = 1.1mA ~ 8.8mA			0.4	V	1
V_{OH}	High-level Output Voltage, V_{DD33} = 2.97V, I_{OH} = -1.1mA ~ -8.8mA	1.85			V	1

1.8V CMOS - Conditions: V_{DD33} = 1.8V +/- 10%

Symbol	Parameter (Condition)	Min	Typ	Max	Units	Note
V_{IL}	Low-level Input Voltage (V_{DD33} = 1.62V)	-0.3		0.3 * V_{DD33}	V	
V_{IH}	High-level Input Voltage (V_{DD33} = 1.98V)	0.7 * V_{DD33}		1.98	V	
V_T	Switching Threshold (Non-Schmitt triggered)		0.85		V	
V_{T-}	Switching Threshold (Schmitt triggered – negative edge)	0.3 * V_{DD33}	0.65		V	
V_{T+}	Switching Threshold (Schmitt triggered – positive edge)		1.08	0.7 * V_{DD33}	V	
R_{PU}	Pull Up Resistance	80	200	510	KOhm	
R_{PD}	Pull Down Resistance	80	210	510	KOhm	
V_{OL}	Low-level Output Voltage, V_{DD33} = 1.98V, I_{OL} = 0.7mA ~ 5.6mA			0.4	V	1
V_{OH}	High-level Output Voltage, V_{DD33} = 1.62V, I_{OH} = -0.7mA ~ -5.6mA	0.75 * V_{DD33}			V	1

Current, Leakage, and Capacitance - Conditions: V_{DD33} = 3.3V

Symbol	Parameter (Condition)	Min	Typ	Max	Units	Note
I_{DDD18}	1.8V Supply Operating Current (f_S = 48 kHz)		11.6		mA	
I_{DDS18}	1.8V Supply Operating Current (Standby)		<10		uA	
I_{DDD33}	3.3V Supply Operating Current (f_S = 48 kHz)		200		uA	2
I_{DDS33}	3.3V Supply Operating Current (Standby)		<10		uA	3
I_{IH}, I_{IL}	Input Leakage Current (V_{in} = V_{DD33} or 0V)	-10	+/- 1	10	uA	
I_{OZ}	Tristate Output Leakage Current (V_{in} = V_{DD33} or 0V)	-10	+/- 1	10	uA	
C_{IN}	Input Capacitance			10	pF	
C_O	Output Capacitance			10	pF	
C_{load}	Load Capacitance			7	pF	

Note 1: Each output has eight programmable drive strength values. The appropriate current load should be used for the corresponding drive strength programmed. For example, with V_{DD33} = 3.3V, an output buffer programmed to use the weakest drive strength should apply a 2mA source or sink current when measuring V_{OL} or V_{OL}. If the next strongest drive strength is programmed, a 4mA source or sink current should be applied. Lower drive strengths result when using lower V_{DD33} values.

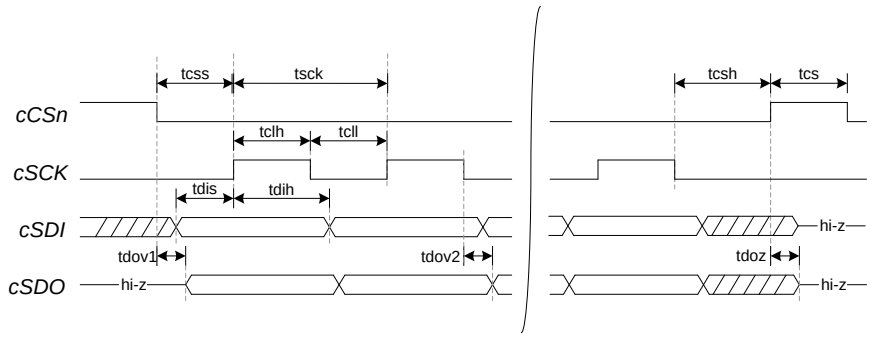
Note 2: SPI and SIB inactive. All pins with pull-ups / pulldowns enabled are not being actively driven by another device.

Note 3: Audio Data Bus, SPI and SIB all inactive. All pins with pull-ups / pulldowns enabled are not being actively driven by another device.

8.4 AC Electrical Characteristics

8.4.1 SPI Configuration Timing Requirements

Timing



Symbol	Parameter (SPI Input)	Min	Max	Units	Note
tsck	SPI Port Clock Period	40		nS	
fsck	SPI Port Clock Frequency (1/tsck)		25	MHz	
tcll	cSCK low time	10		nS	
tclh	cSCK high time	10		nS	
tcss	cCSn falling to cSCK rising time	7		nS	
tcsh	cSCK falling to cCSn rising time	10		nS	
tcs	cCSn high time	50		nS	
tdis	cSDI setup time	7		nS	
tdih	cSDI hold time	10		nS	
tdov1	cCSn falling to cSDO valid time		10	nS	
tdov2	cSCK falling to cSDO valid time		10	nS	
tdoz	cCSn rising to SDO high-Z time		10	nS	

Table 8-1 - SPI Interface Bus Timing

8.4.2 SIB Timing Requirements

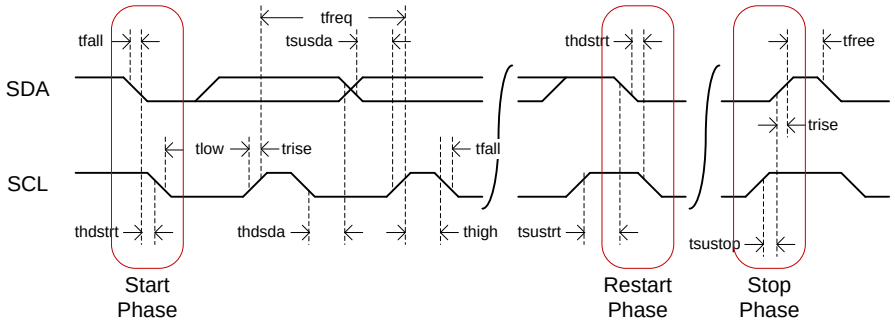
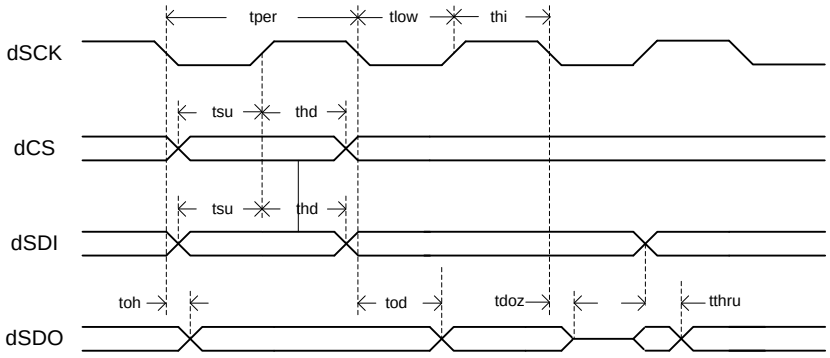


Figure 8-1 - Serial Interface Bus Timing Diagram

Symbol	Parameter (SPI Input)	Min	Max	Units	Note
tfreq	SCLK Frequency		400	kHz	
thdstrt	Start Phase Hold Time SCL Falling after SDA Falling	160		ns	
tsustrt	Restart Phase Setup Time SCL Rising to SDA Falling	160		ns	
tsustop	Stop Phase Setup Time SCL Rising to SDA Rising	160		ns	
tfall	SDA / SCL Fall Time	20	160	ns	
trise	SDA / SCL Rise Time	20	160	ns	
tlow	SCL Low Time	320		ns	
thigh	SCL High Time	120		ns	
tsusda	Data Phase Setup Time SDA to SCL Rising	10		ns	
thdsda	Data Phase Hold Time Data Valid after SCL Falling	160		ns	
tfree	SDA High Time during Bus Idle	1.3		us	

Table 8-2 - Serial Interface Bus Timing

8.4.3 Audio Data Path Timing Requirements



Note: dSCK polarity is inverted if dsck_pol=0

Figure 8-2 - Audio Data Path Timing Diagram 1

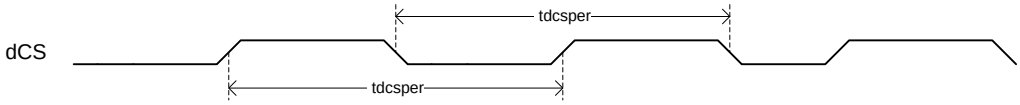


Figure 8-3 - Audio Data Path Timing Diagram 2

Symbol	Parameter(SPI Output)	Min	Max	Units	Note
tfreq	dSCK Frequency		25	MHz	
tper	dSCK Period	40		ns	
tsu	dCS / dSDI Setup to dSCK Rising	3		ns	
tdh	dCS / dSDI Hold from dSCK Rising	5		ns	
toh	dSDO Output Hold from dSCK Falling	0		ns	
tod	dSDOn Delay from dSCK Falling (normal mode)		6	ns	
tdoz	dSDOn Tristate from dSCK Falling		6	ns	
tthru	dSDOn Delay from dSDI (passthru mode)	8		ns	
tdcsper	dCS Rising to Rising or Falling to Falling	20		us	
tdcsfreq	dCS Frequency (1/tdcsper)		50	kHz	

Table 8-3 - Audio Data Path Timing

8.4.4 Miscellaneous Timing Requirements

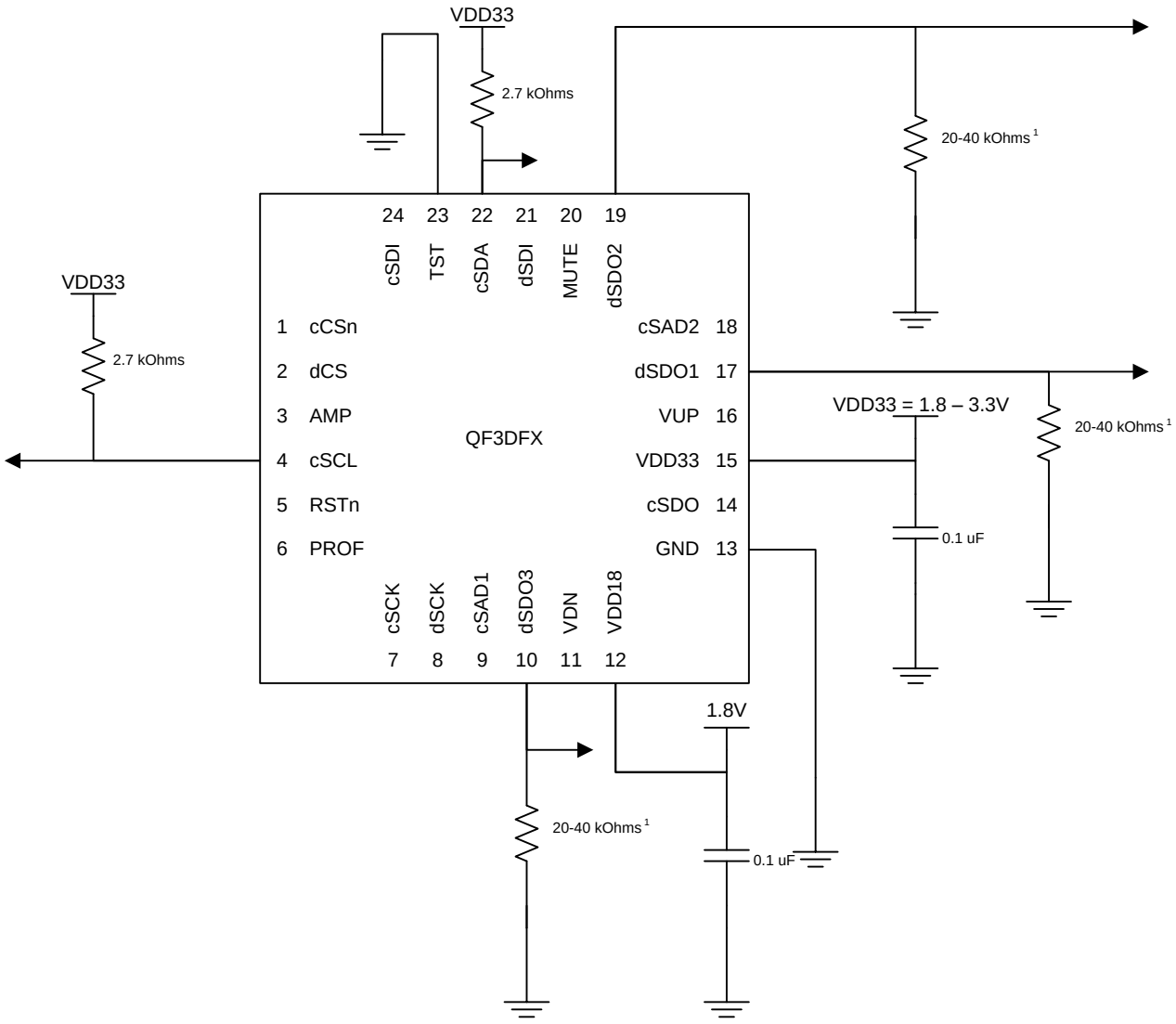
Symbol	Parameter(SPI Output)	Min	Max	Units	Note
trstl	RSTn low after VDD33 and VDD18 Valid	50		ns	

Table 8-4 – Miscellaneousl Timing Requirements

9 CONNECTION DIAGRAMS

9.1 Electrical Connections

The diagram below illustrates recommended components and their values in a typical system.



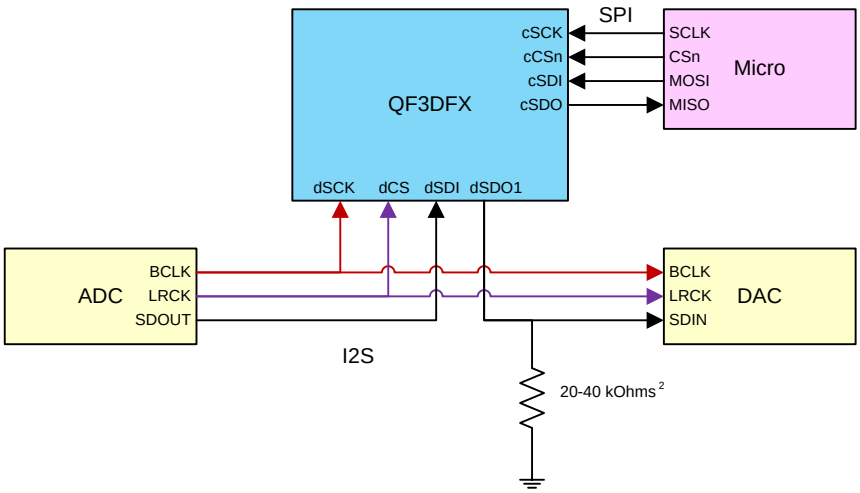
1. A weak pulldown resistor is recommended on each dSDOn line as the dSDOn pins tristate when filt_en and din_pt in the CONTROL register are both low.

Figure 9-1 Recommended Electrical Connection

9.2 Example Systems

9.2.1 SPI-Based Microcontroller

The diagram below illustrates a system with separate ADC, DAC, and Micro (used to boot and program from).



Note: The QF3DFX is always an I2S Slave, but any other device may control the Bit Clock (BCLK) and Word Select (LRCK) lines.

Figure 9-2 QF3DFX With SPI-Based Microcontroller

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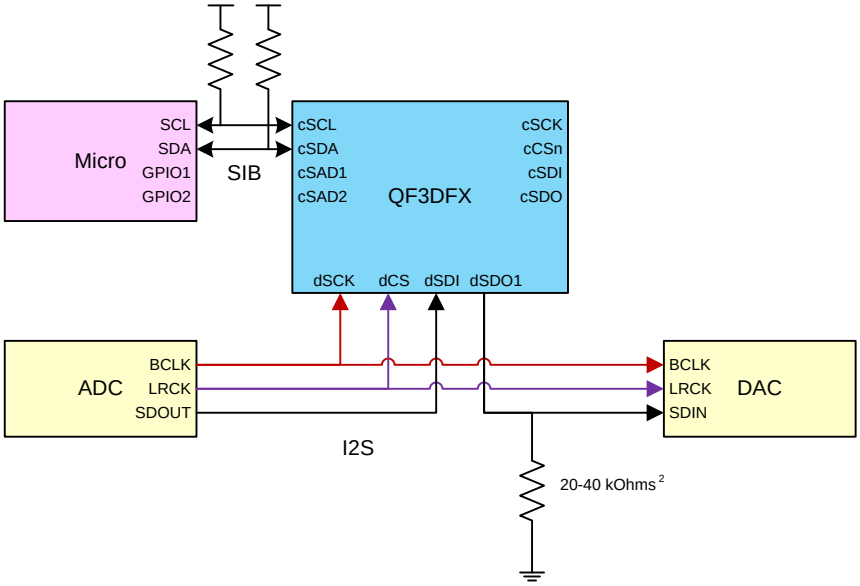
9.2.2 SIB-Based Microcontroller

The diagram below illustrates a system with separate ADC, DAC, and SIB-Based (2-Wire Interface) Micro. The micro provides all boot code and programming of the QF3DFX.

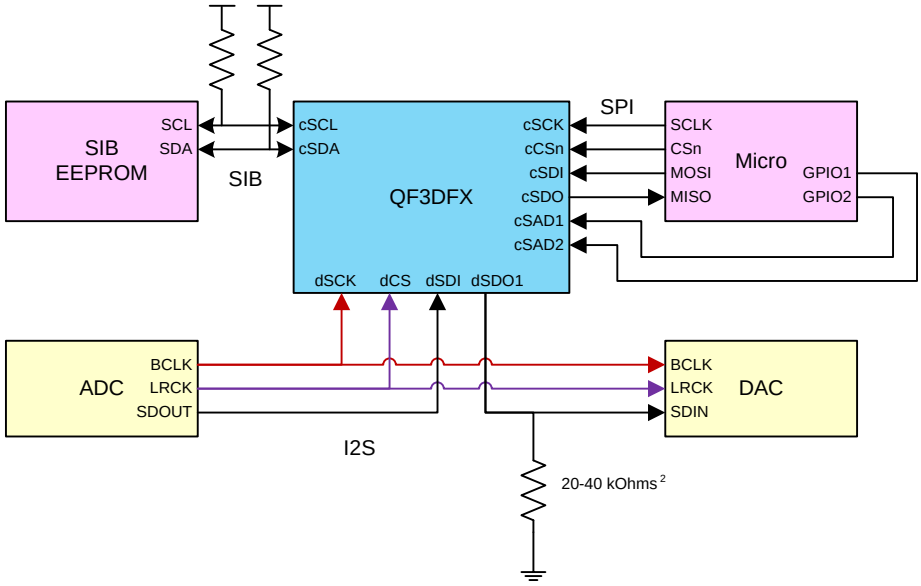


Note: The QF3DFX is always an I2S Slave, but any other device may control the Bit Clock (BCLK) and Word Select (LRCK) lines.

Figure 9-3 QF3DFX With SIB-Based Microcontroller

9.2.3 SPI-Based Microcontroller with QF3DFX Boot EEPROM

The diagram below illustrates a system with separate ADC, DAC, and SPI-based Micro. The QF3DFX gets its initial boot code from an SIB-based EEPROM, but most subsequent programming comes from the SPI-based Micro.



Note: The QF3DFX is always an I2S Slave, but any other device may control the Bit Clock (BCLK) and Word Select (LRCK) lines.

Figure 9-4 QF3DFX With SPI-Based Microcontroller and Boot EEPROM

10 PACKAGING INFORMATION

10.1 Package Assembly

The QF3DFX is offered in a “green” package (RoHS & no Sb/Br), assembled with enhanced environmentally compatible Pb-free and halide-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 260°C during printed circuit board assembly.

4 x 4 x 0.9mm, VQFN 24, 0.8 mm Pull Back Lead (JEDEC)

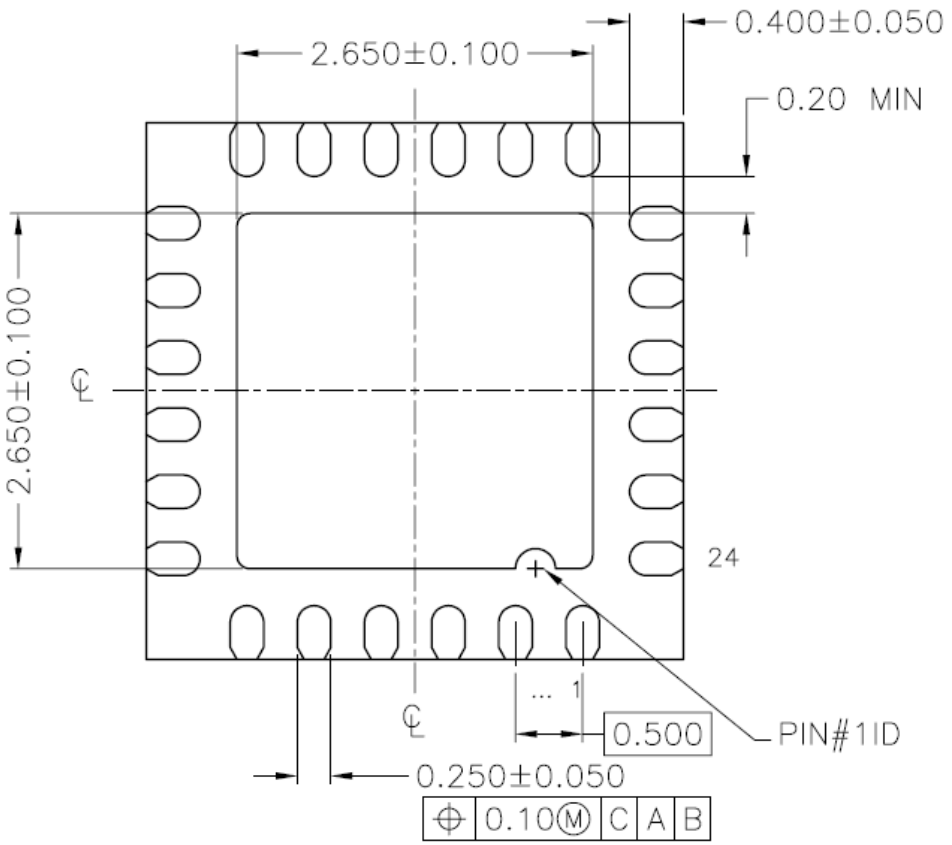


Figure 10-1- VQFN 24, Bottom View

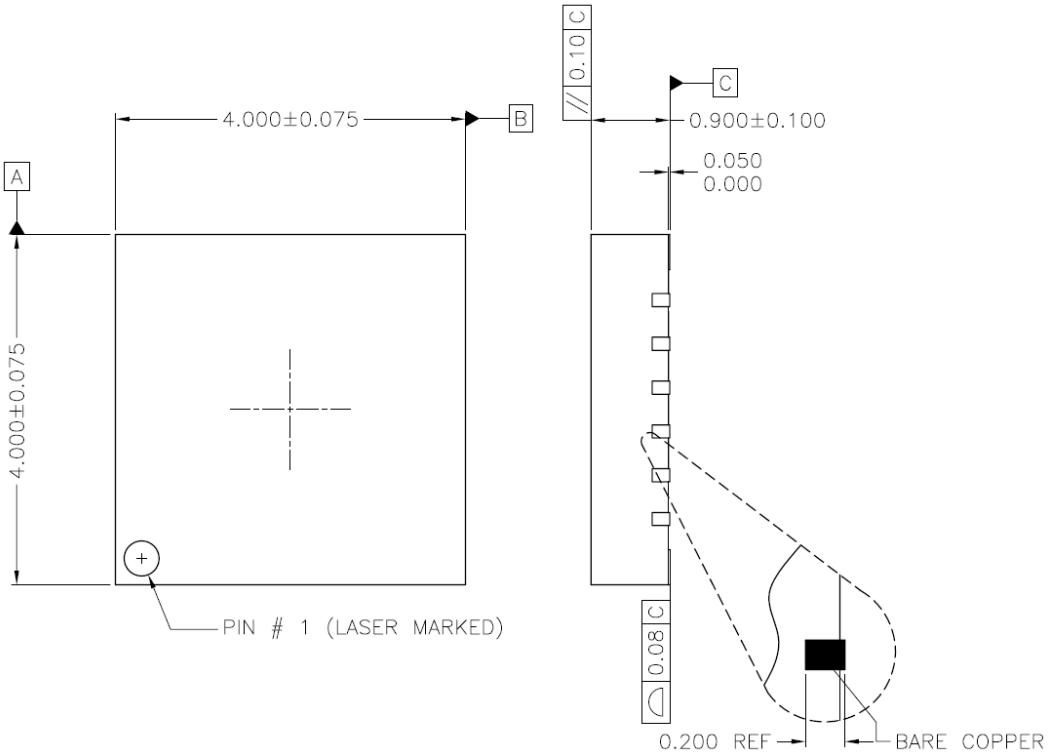


Figure 10-2 - VQFN 24, Top / Side View

Notes:

1. Dimensions are in millimeters.
2. Interpret dimensions and tolerance per ASME Y14.5M-1994

11 ORDERING INFORMATION

Device	Package
QF3DFX0QN02400T	24-Pin QFN - Tape & Reel (Reel qty 1000)
QF3DFX-DK	Evaluation Platform

1024 S. Greenville Ave
Suite 130
Allen, TX 75002-3344

Telephone: (214) 547-0460
Fax: (214) 547-0481

For inquiries, please contact Quickfilter at the above address,

Or visit our website:
http://www.quickfiltertech.com