



**Features**

- UL Certified No. E209204
- 600 V - 20 A 3 - Phase IGBT Inverter Bridge Including Control ICs for Gate Driving and Protection
- Three Separate Open - Emitter Pins from Low Side IGBTs for Three Leg Current Sensing
- Single-Grounded Power Supply Thanks to Built-in HVIC
- Typical Switching Frequency of 15 kHz
- Built-in Thermistor for Temperature Monitoring
- Inverter Power Rating of 1.5 kW / 100~253 VAC
- Isolation Rating of 2500 Vrms / min.
- Low Thermal Resistance by Using Ceramic Substrate
- Adjustable Current Protection Level by Changing the Value of Series Resistor Connected to the Emitters of Sense-IGBTs

**Applications**

- Motion Control - Home Appliance / Industrial Motor

**General Description**

FSAM20SH60A Is A Motion SPM® 2 Series that Fairchild Has Developed to Provide A Very Compact and Low Cost, yet High Performance Inverter Solution for AC Motor Drives in Low-Power Applications Such as Air Conditioners. It Combines Optimized Circuit Protections and Drive Matched to Low-Loss IGBTs. Effective Over-Current Protection Is Realized Through Advanced Current Sensing IGBTs. The System Reliability Is Further Enhanced by The Built-in Thermistor and Integrated Under-Voltage Lock-Out Protection. In Addition The Incorporated HVIC Facilitates The Use of Single-Supply Voltage Without Any Negative Bias. Inverter Leg Current Sensing Can Be Implemented Because of Three Separate Negative DC Terminals.

**Related Source**

- [AN-9043 : Motion SPM® 2 Series User's Guide](#)

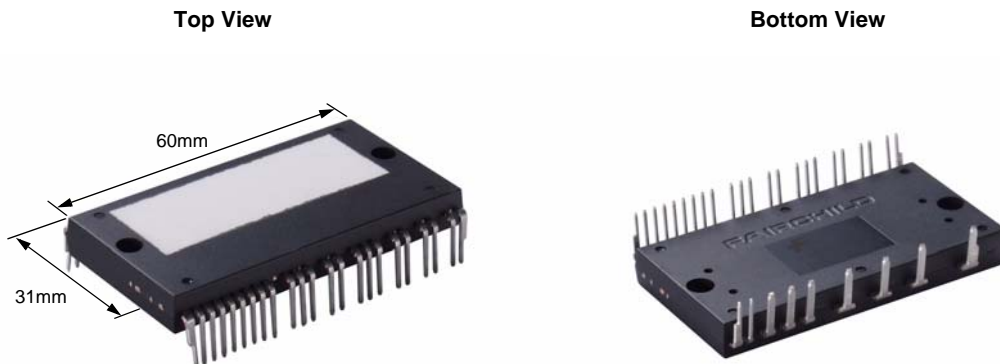


Fig. 1.

**Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Packing Type	Quantity
FSAM20SH60A	FSAM20SH60A	S32AA-032	-	RAIL	8

### Integrated Power Functions

- 600 V-20 A IGBT inverter for 3 - phase DC/AC power conversion (Please refer to Fig. 3)

### Integrated Drive, Protection and System Control Functions

- For inverter high-side IGBTs: Gate drive circuit, High voltage isolated high-speed level shifting  
Control circuit under-voltage (UV) protection  
Note) Available bootstrap circuit example is given in Figs. 14 and 15.
- For inverter low-side IGBTs: Gate drive circuit, Short-Circuit (SC) protection  
Control supply circuit under-voltage (UV) protection
- Temperature Monitoring: System over-temperature monitoring using built-in thermistor  
Note) Available temperature monitoring circuit is given in Fig. 15.
- Fault signaling: Corresponding to a SC fault (Low-side IGBTs) or a UV fault (Low-side control supply circuit)
- Input interface: Active - Low Interface, Can Work with 3.3/5 V Logic

### Pin Configuration

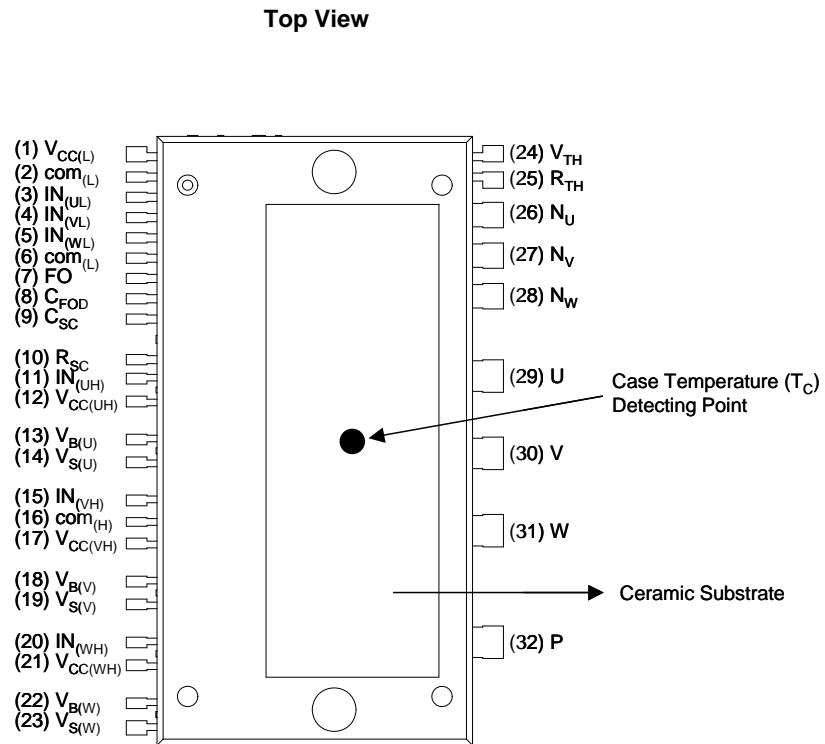


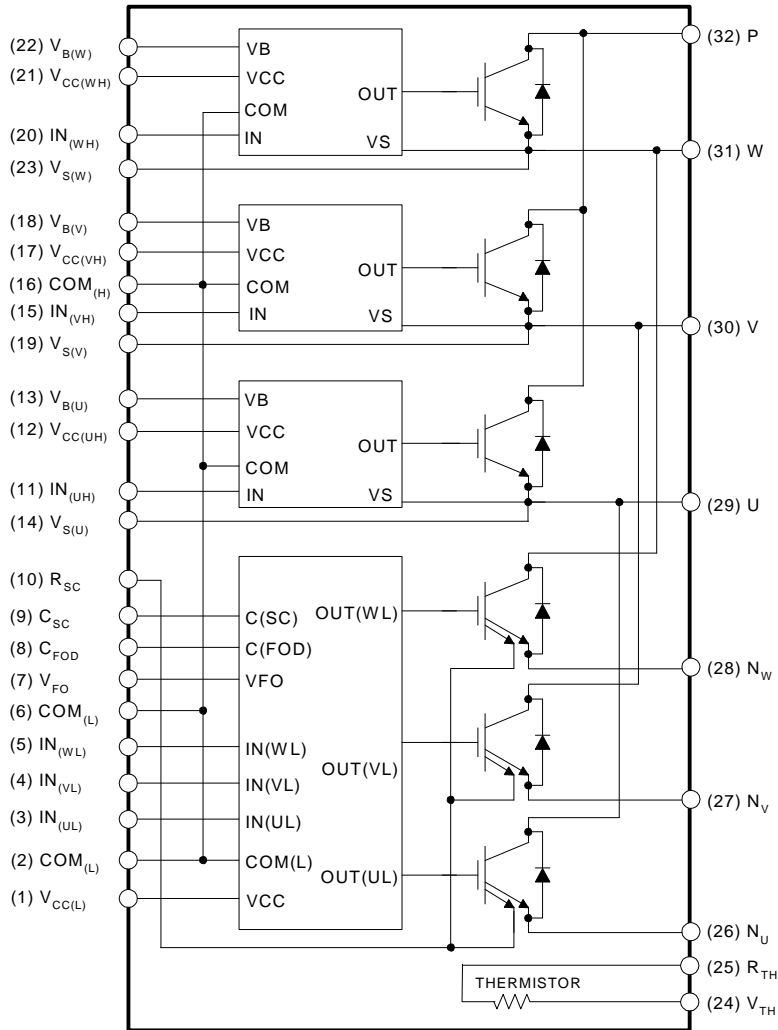
Fig. 2.

## Pin Descriptions

Pin Number	Pin Name	Pin Description
1	$V_{CC(L)}$	Low-side Common Bias Voltage for IC and IGBTs Driving
2	$COM_{(L)}$	Low-side Common Supply Ground
3	$IN_{(UL)}$	Signal Input for Low-side U Phase
4	$IN_{(VL)}$	Signal Input for Low-side V Phase
5	$IN_{(WL)}$	Signal Input for Low-side W Phase
6	$COM_{(L)}$	Low-side Common Supply Ground
7	$V_{FO}$	Fault Output
8	$C_{FOD}$	Capacitor for Fault Output Duration Time Selection
9	$C_{SC}$	Capacitor (Low-pass Filter) for Short-Circuit Current Detection Input
10	$R_{SC}$	Resistor for Short-Circuit Current Detection
11	$IN_{(UH)}$	Signal Input for High-side U Phase
12	$V_{CC(UH)}$	High-side Bias Voltage for U Phase IC
13	$V_{B(U)}$	High-side Bias Voltage for U Phase IGBT Driving
14	$V_{S(U)}$	High-side Bias Voltage Ground for U Phase IGBT Driving
15	$IN_{(VH)}$	Signal Input for High-side V Phase
16	$COM_{(H)}$	High-side Common Supply Ground
17	$V_{CC(VH)}$	High-side Bias Voltage for V Phase IC
18	$V_{B(V)}$	High-side Bias Voltage for V Phase IGBT Driving
19	$V_{S(V)}$	High-side Bias Voltage Ground for V Phase IGBT Driving
20	$IN_{(WH)}$	Signal Input for High-side W Phase
21	$V_{CC(WH)}$	High-side Bias Voltage for W Phase IC
22	$V_{B(W)}$	High-side Bias Voltage for W Phase IGBT Driving
23	$V_{S(W)}$	High-side Bias Voltage Ground for W Phase IGBT Driving
24	$V_{TH}$	Thermistor Bias Voltage
25	$R_{TH}$	Series Resistor for the Use of Thermistor (Temperature Detection)
26	$N_U$	Negative DC-Link Input for U Phase
27	$N_V$	Negative DC-Link Input for V Phase
28	$N_W$	Negative DC-Link Input for W Phase
29	U	Output for U Phase
30	V	Output for V Phase
31	W	Output for W Phase
32	P	Positive DC-Link Input

Internal Equivalent Circuit and Input/Output Pins

Bottom View



Note:

- 1) Inverter low-side is composed of three sense-IGBTs including freewheeling diodes for each IGBT and one control IC which has gate driving, current sensing and protection functions.
- 2) Inverter power side is composed of four inverter dc-link input pins and three inverter output pins.
- 3) Inverter high-side is composed of three normal-IGBTs including freewheeling diodes and three drive ICs for each IGBT.

Fig. 3.

## Absolute Maximum Ratings ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)

### Inverter Part

Item	Symbol	Condition	Rating	Unit
Supply Voltage	$V_{PN}$	Applied between P- $N_U$ , $N_V$ , $N_W$	450	V
Supply Voltage (Surge)	$V_{PN(\text{Surge})}$	Applied between P- $N_U$ , $N_V$ , $N_W$	500	V
Collector-Emitter Voltage	$V_{CES}$		600	V
Each IGBT Collector Current	$\pm I_C$	$T_C = 25^\circ\text{C}$	20	A
Each IGBT Collector Current	$\pm I_C$	$T_C = 100^\circ\text{C}$	14	A
Each IGBT Collector Current (Peak)	$\pm I_{CP}$	$T_C = 25^\circ\text{C}$ , Instantaneous Value (Pulse)	40	A
Collector Dissipation	$P_C$	$T_C = 25^\circ\text{C}$ per One Chip	59	W
Operating Junction Temperature	$T_J$	(Note 1)	-20 ~ 125	$^\circ\text{C}$

**Note:**

1. It would be recommended that the average junction temperature should be limited to  $T_J \leq 125^\circ\text{C}$  ( $@T_C \leq 100^\circ\text{C}$ ) in order to guarantee safe operation.

### Control Part

Item	Symbol	Condition	Rating	Unit
Control Supply Voltage	$V_{CC}$	Applied between $V_{CC(UH)}$ , $V_{CC(VH)}$ , $V_{CC(WH)} - \text{COM}_{(H)}$ , $V_{CC(L)} - \text{COM}_{(L)}$	20	V
High-side Control Bias Voltage	$V_{BS}$	Applied between $V_{B(U)} - V_{S(U)}$ , $V_{B(V)} - V_{S(V)}$ , $V_{B(W)} - V_{S(W)}$	20	V
Input Signal Voltage	$V_{IN}$	Applied between $IN_{(UH)}$ , $IN_{(VH)}$ , $IN_{(WH)} - \text{COM}_{(H)}$ $IN_{(UL)}$ , $IN_{(VL)}$ , $IN_{(WL)} - \text{COM}_{(L)}$	-0.3 ~ $V_{CC}+0.3$	V
Fault Output Supply Voltage	$V_{FO}$	Applied between $V_{FO} - \text{COM}_{(L)}$	-0.3 ~ $V_{CC}+0.3$	V
Fault Output Current	$I_{FO}$	Sink Current at $V_{FO}$ Pin	5	mA
Current Sensing Input Voltage	$V_{SC}$	Applied between $C_{SC} - \text{COM}_{(L)}$	-0.3 ~ $V_{CC}+0.3$	V

### Total System

Item	Symbol	Condition	Rating	Unit
Self Protection Supply Voltage Limit (Short-Circuit Protection Capability)	$V_{PN(\text{PROT})}$	$V_{CC} = V_{BS} = 13.5 \sim 16.5 \text{ V}$ $T_J = 125^\circ\text{C}$ , Non-repetitive, less than $6\mu\text{s}$	400	V
Module Case Operation Temperature	$T_C$	Note Fig.2	-20 ~ 100	$^\circ\text{C}$
Storage Temperature	$T_{STG}$		-20 ~ 125	$^\circ\text{C}$
Isolation Voltage	$V_{ISO}$	60Hz, Sinusoidal, AC 1 minute, Connection Pins to Heat-sink Plate	2500	$V_{\text{rms}}$

## Absolute Maximum Ratings

### Thermal Resistance

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Junction to Case Thermal Resistance	$R_{th(j-c)Q}$	Each IGBT under Inverter Operating Condition	-	-	2.1	°C/W
	$R_{th(j-c)F}$	Each FWDi under Inverter Operating Condition	-	-	3.3	°C/W
Contact Thermal Resistance	$R_{th(c-f)}$	Ceramic Substrate (per 1 Module) Thermal Grease Applied (Note 3)	-	-	0.06	°C/W

**Note:**

- For the measurement point of case temperature ( $T_C$ ), please refer to Fig. 2.
- The thickness of thermal grease should not be more than 100µm.

### Electrical Characteristics ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)

#### Inverter Part

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
Collector - Emitter Saturation Voltage	$V_{CE(SAT)}$	$V_{CC} = V_{BS} = 15\text{ V}$ $V_{IN} = 0\text{ V}$	$I_C = 20\text{ A}, T_J = 25^\circ\text{C}$	-	-	2.5	V
			$I_C = 20\text{ A}, T_J = 125^\circ\text{C}$	-	-	2.6	V
FWDi Forward Voltage	$V_{FM}$	$V_{IN} = 5\text{ V}$	$I_C = 20\text{ A}, T_J = 25^\circ\text{C}$	-	-	2.5	V
			$I_C = 20\text{ A}, T_J = 125^\circ\text{C}$	-	-	2.3	V
Switching Times	$t_{ON}$	$V_{PN} = 300\text{ V}, V_{CC} = V_{BS} = 15\text{ V}$ $I_C = 20\text{ A}, T_J = 25^\circ\text{C}$ $V_{IN} = 5\text{ V} \leftrightarrow 0\text{ V}$ , Inductive Load (High, Low-side)	-	0.35	-	us	
	$t_{C(ON)}$		-	0.16	-	us	
	$t_{OFF}$		-	0.75	-	us	
	$t_{C(OFF)}$		-	0.23	-	us	
	$t_{rr}$		(Note 4)	-	0.13	-	us
Collector - Emitter Leakage Current	$I_{CES}$	$V_{CE} = V_{CES}, T_J = 25^\circ\text{C}$	-	-	250	µA	

**Note:**

- $t_{ON}$  and  $t_{OFF}$  include the propagation delay time of the internal drive IC.  $t_{C(ON)}$  and  $t_{C(OFF)}$  are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Fig. 4.

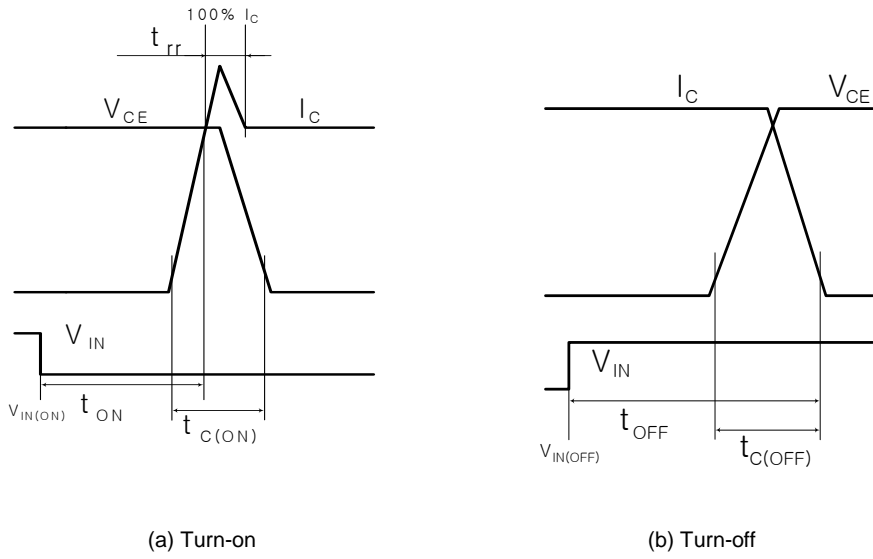


Fig. 4. Switching Time Definition

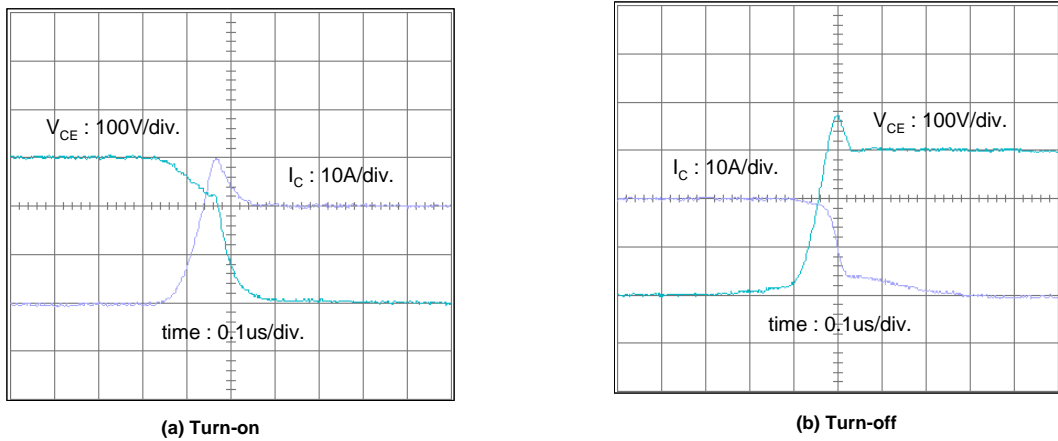


Fig. 5. Experimental Results of Switching Waveforms  
 Test Condition:  $V_{dc}=300V$ ,  $V_{cc}=15V$ ,  $L=500\mu H$  (Inductive Load),  $T_j=25^\circ C$

## Electrical Characteristics (T<sub>J</sub> = 25°C, Unless Otherwise Specified)

### Control Part

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Control Supply Voltage	V <sub>CC</sub>	Applied between V <sub>CC(UH)</sub> , V <sub>CC(VH)</sub> , V <sub>CC(WH)</sub> , V <sub>CC(L)</sub> - COM	13.5	15	16.5	V
High-side Bias Voltage	V <sub>BS</sub>	Applied between V <sub>B(U)</sub> - V <sub>S(U)</sub> , V <sub>B(V)</sub> - V <sub>S(V)</sub> , V <sub>B(W)</sub> - V <sub>S(W)</sub>	13.5	15	16.5	V
Quiescent V <sub>CC</sub> Supply Current	I <sub>QCCL</sub>	V <sub>CC</sub> = 15 V I <sub>N(UH, VL, WL)</sub> = 5 V			26	mA
	I <sub>QCCH</sub>	V <sub>CC</sub> = 15 V I <sub>N(UH, VH, WH)</sub> = 5 V			130	µA
Quiescent V <sub>BS</sub> Supply Current	I <sub>QBS</sub>	V <sub>BS</sub> = 15 V I <sub>N(UH, VH, WH)</sub> = 5 V			420	µA
Fault Output Voltage	V <sub>FOH</sub>	V <sub>SC</sub> = 0 V, V <sub>FO</sub> Circuit: 4.7 kΩ to 5 V Pull-up	4.5	-	-	V
	V <sub>FOL</sub>	V <sub>SC</sub> = 1 V, V <sub>FO</sub> Circuit: 4.7 kΩ to 5 V Pull-up	-	-	1.1	V
PWM Input Frequency	f <sub>PWM</sub>	T <sub>C</sub> ≤ 100°C, T <sub>J</sub> ≤ 125°C	-	15	-	kHz
Allowable Input Signal Blanking Time considering Leg Arm-short	t <sub>dead</sub>	-20°C ≤ T <sub>C</sub> ≤ 100°C	3	-	-	µs
Short-Circuit Trip Level	V <sub>SC(ref)</sub>	V <sub>CC</sub> = 15 V (Note 5)	0.45	0.51	0.56	V
Sensing Voltage of IGBT Current	V <sub>SEN</sub>	T <sub>C</sub> = 25°C, @ R <sub>SC</sub> = 50 Ω, R <sub>SU</sub> = R <sub>SV</sub> = R <sub>SW</sub> = 0 Ω and I <sub>C</sub> = 30 A (Note Fig. 7)	0.45	0.51	0.56	V
Supply Circuit Under-Voltage Protection	UV <sub>CCD</sub>	Detection Level	11.5	12	12.5	V
	UV <sub>CCR</sub>	Reset Level	12	12.5	13	V
	UV <sub>BSD</sub>	Detection Level	7.3	9.0	10.8	V
	UV <sub>BSR</sub>	Reset Level	8.6	10.3	12	V
Fault Output Pulse Width	t <sub>FOD</sub>	C <sub>FOD</sub> = 33 nF (Note 6)	1.4	1.8	2.0	ms
ON Threshold Voltage	V <sub>IN(ON)</sub>	High-Side			0.8	V
OFF Threshold Voltage	V <sub>IN(OFF)</sub>		3.0	-	-	V
ON Threshold Voltage	V <sub>IN(ON)</sub>	Low-Side			0.8	V
OFF Threshold Voltage	V <sub>IN(OFF)</sub>		3.0	-	-	V
Resistance of Thermistor	R <sub>TH</sub>	@ T <sub>TH</sub> = 25°C (Note Fig. 6)	-	50	-	kΩ
		@ T <sub>TH</sub> = 100°C (Note Fig. 6)	-	3.4	-	kΩ

**Note:**

- Short-circuit current protection is functioning only at the low-sides. It would be recommended that the value of the external sensing resistor (R<sub>SC</sub>) should be selected around 50 Ω in order to make the SC trip-level of about 30A at the shunt resistors (R<sub>SU</sub>, R<sub>SV</sub>, R<sub>SW</sub>) of 0Ω. For the detailed information about the relationship between the external sensing resistor (R<sub>SC</sub>) and the shunt resistors (R<sub>SU</sub>, R<sub>SV</sub>, R<sub>SW</sub>), please see Fig. 7.
- The fault-out pulse width t<sub>FOD</sub> depends on the capacitance value of C<sub>FOD</sub> according to the following approximate equation : C<sub>FOD</sub> = 18.3 x 10<sup>-6</sup> x t<sub>FOD</sub>[F]
- T<sub>TH</sub> is the temperature of thermistor



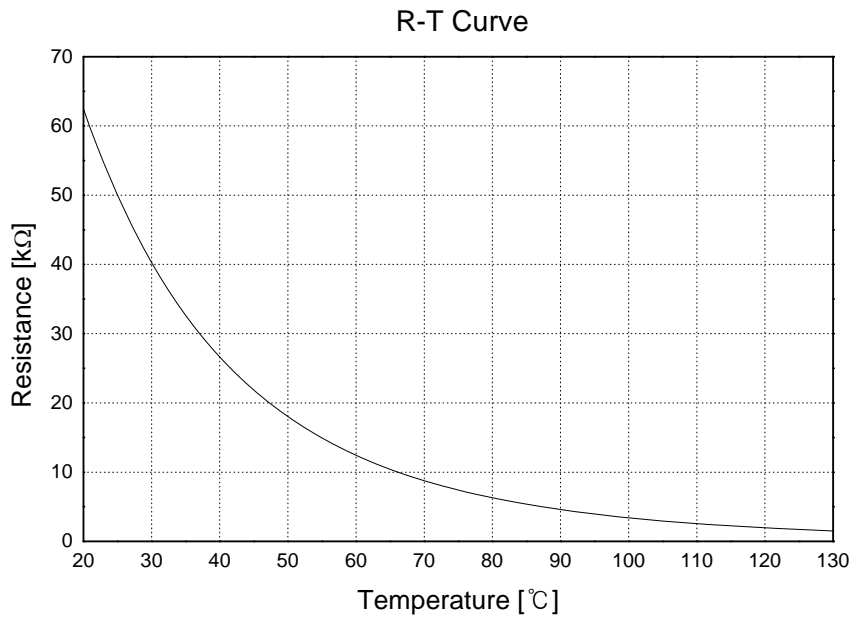


Fig. 6. R-T Curve of The Built-in Thermistor

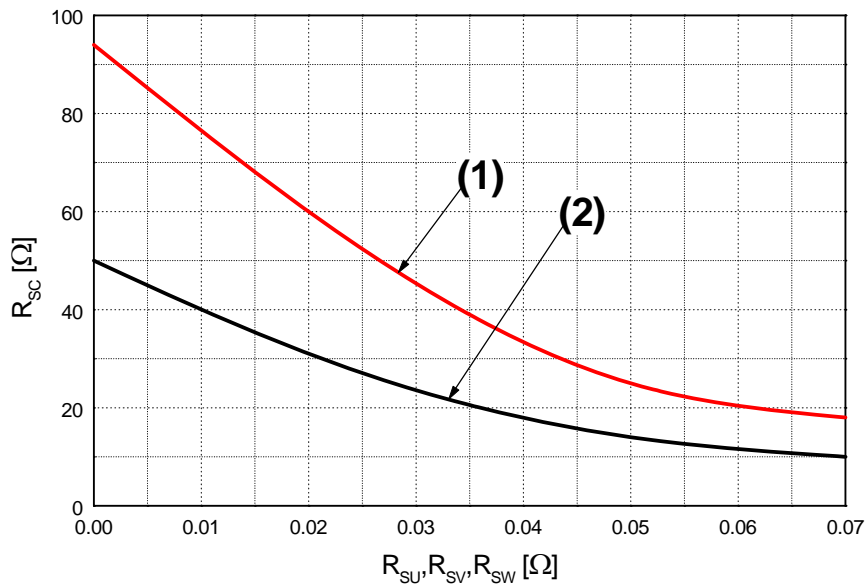
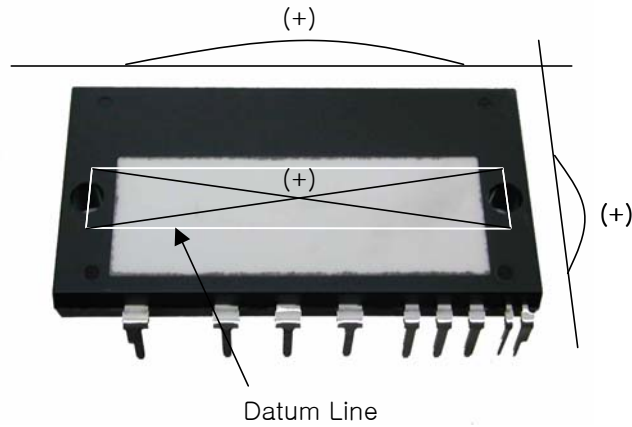


Fig. 7. R<sub>sc</sub> Variation by change of Shunt Resistors (R<sub>SU</sub>, R<sub>SV</sub>, R<sub>SW</sub>) for Short-Circuit Protection  
 (1) @ around 100% Rated Current Trip (I<sub>C</sub> = 20 A)  
 (2) @ around 150% Rated Current Trip (I<sub>C</sub> = 30 A)

### Mechanical Characteristics and Ratings

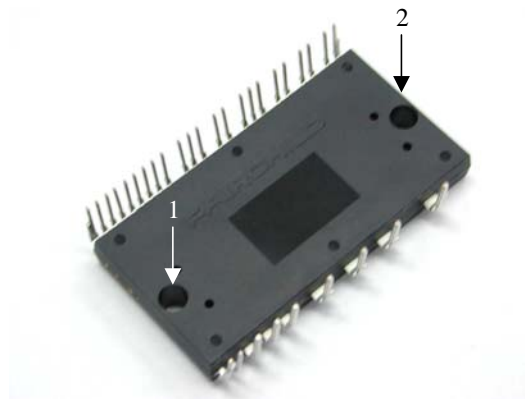
Item	Condition	Limits			Unit	
		Min.	Typ.	Max.		
Mounting Torque	Mounting Screw: M4 (Note 8 and 9)	Recommended 10 Kg•cm	8	10	12	Kg•cm
		Recommended 0.98 N•m	0.78	0.98	1.17	N•m
Ceramic Flatness	Note Fig.8	0	-	+120	um	
Weight		-	35	-	g	



**Fig. 8. Flatness Measurement Position of The Ceramic Substrate**

**Note:**

- 8. Do not make over torque or mounting screws. Much mounting torque may cause ceramic cracks and bolts and Al heat-fin destruction.
- 9. Avoid one side tightening stress. Fig.9 shows the recommended torque order for mounting screws. Uneven mounting can cause the Motion SPM® 2 Package ceramic substrate to be damaged.

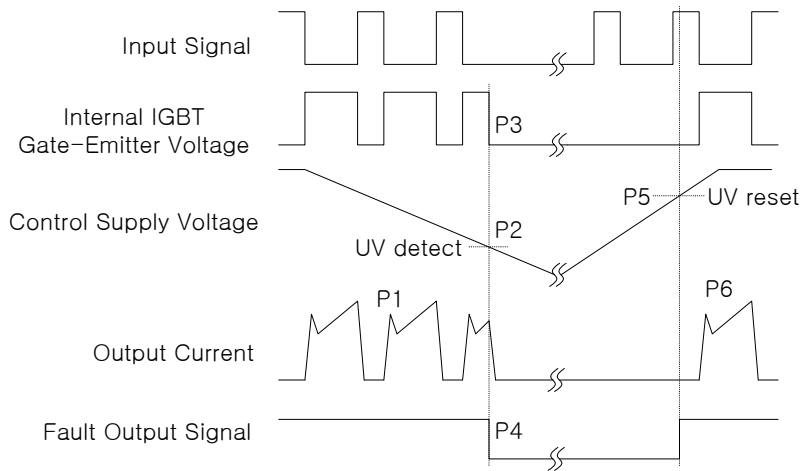


**Fig. 9. Mounting Screws Torque Order**

### Recommended Operating Conditions

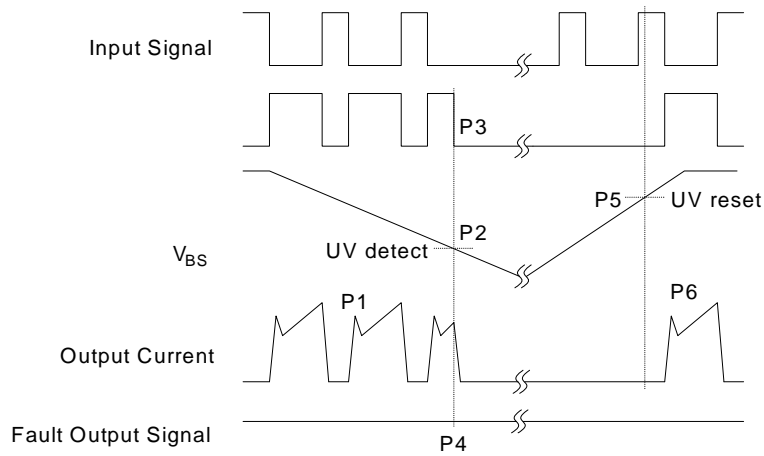
Item	Symbol	Condition	Values			Unit
			Min.	Typ.	Max.	
Supply Voltage	$V_{PN}$	Applied between P - $N_U$ , $N_V$ , $N_W$	-	300	400	V
Control Supply Voltage	$V_{CC}$	Applied between $V_{CC(UH)}$ , $V_{CC(VH)}$ , $V_{CC(WH)}$ - $COM_{(H)}$ , $V_{CC(L)}$ - $COM_{(L)}$	13.5	15	16.5	V
High-side Bias Voltage	$V_{BS}$	Applied between $V_{B(U)}$ - $V_{S(U)}$ , $V_{B(V)}$ - $V_{S(V)}$ , $V_{B(W)}$ - $V_{S(W)}$	13.5	15	16.5	V
Blanking Time for Preventing Arm-short	$t_{dead}$	For Each Input Signal	3	-	-	us
PWM Input Signal	$f_{PWM}$	$T_C \leq 100^\circ C$ , $T_J \leq 125^\circ C$	-	15	-	kHz
Input ON Threshold Voltage	$V_{IN(ON)}$	Applied between $IN_{(UH)}$ , $IN_{(VH)}$ , $IN_{(WH)}$ - $COM_{(H)}$	0 ~ 0.65			V
Input OFF Threshold Voltage	$V_{IN(OFF)}$	Applied between $IN_{(UL)}$ , $IN_{(VL)}$ , $IN_{(WL)}$ - $COM_{(L)}$	4 ~ 5.5			V

### Time Charts of Protective Function



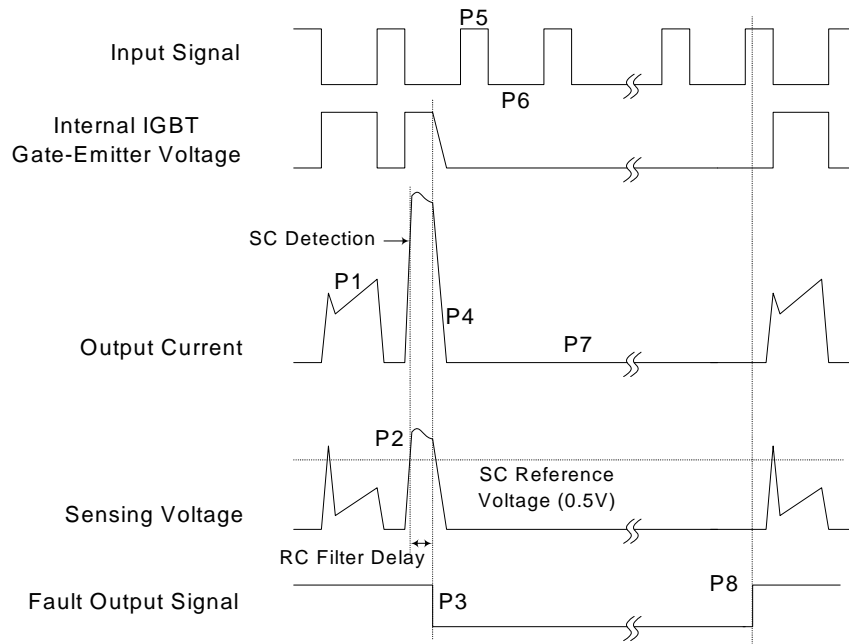
- P1 : Normal operation - IGBT ON and conducting current
- P2 : Under-Voltage detection
- P3 : IGBT gate interrupt
- P4 : Fault signal generation
- P5 : Under-Voltage reset
- P6 : Normal operation - IGBT ON and conducting current

**Fig. 10. Under-Voltage Protection (Low-side)**



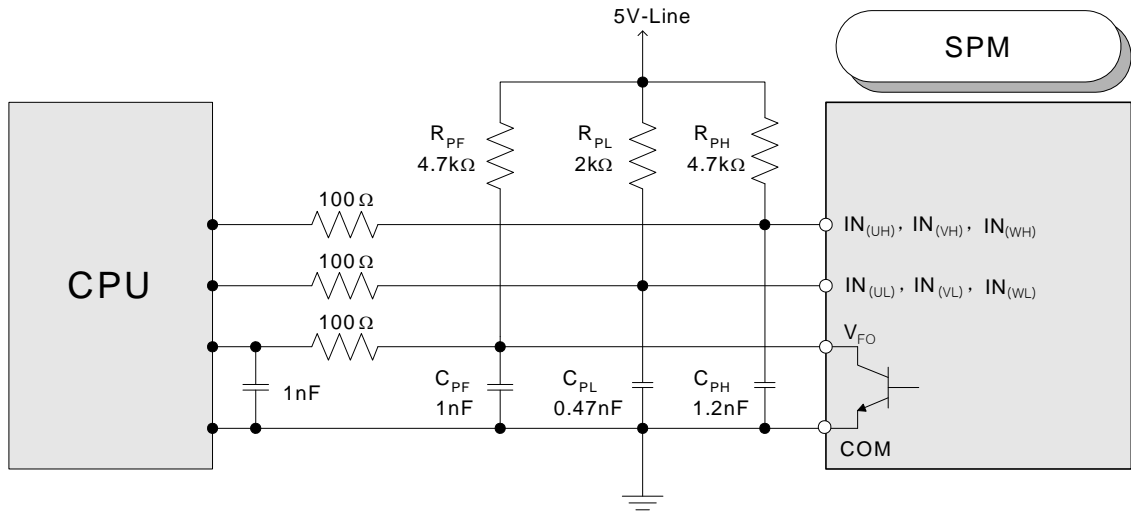
- P1 : Normal operation - IGBT ON and conducting current
- P2 : Under-Voltage detection
- P3 : IGBT gate interrupt
- P4 : No fault signal
- P5 : Under-Voltage reset
- P6 : Normal operation - IGBT ON and conducting current

**Fig. 11. Under-Voltage Protection (High-side)**



- P1 : Normal operation - IGBT ON and conducting current
- P2 : Short-Circuit current detection
- P3 : IGBT gate interrupt / Fault signal generation
- P4 : IGBT is slowly turned off
- P5 : IGBT OFF signal
- P6 : IGBT ON signal - but IGBT cannot be turned on during the fault Output activation
- P7 : IGBT OFF state
- P8 : Fault Output reset and normal operation start

**Fig. 12. Short-Circuit Current Protection (Low-side Operation only)**

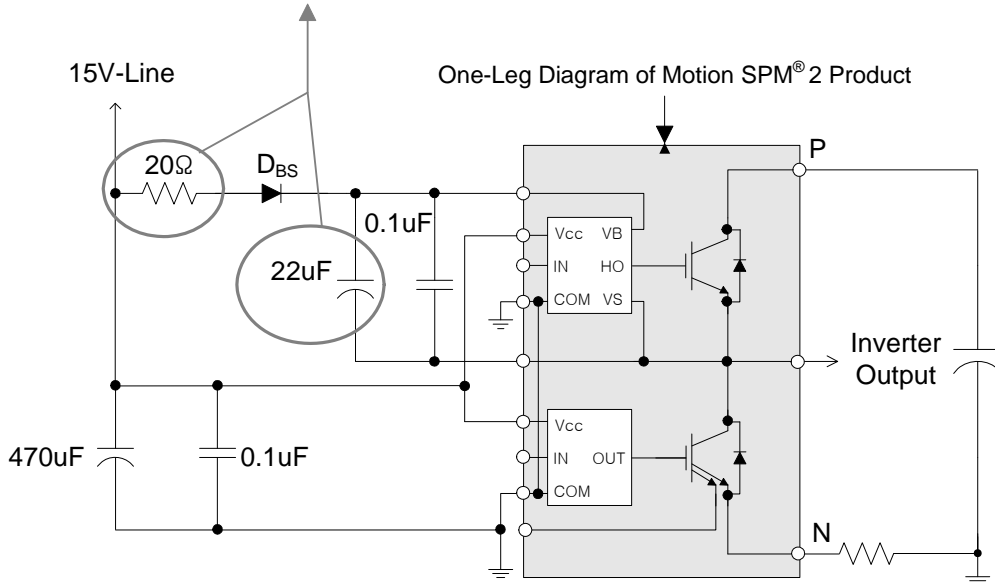


**Note:**

- 1) It would be recommended that by-pass capacitors for the gating input signals,  $IN_{(UL)}$ ,  $IN_{(VL)}$ ,  $IN_{(WL)}$ ,  $IN_{(UH)}$ ,  $IN_{(VH)}$  and  $IN_{(WH)}$  should be placed on the Motion SPM® 2 Product pins and on the both sides of CPU and Motion SPM 2 Product for the fault output signal,  $V_{FO}$ , as close as possible.
- 2) The logic input is compatible with standard CMOS or LSTTL outputs.
- 3)  $R_{PL}C_{PL}/R_{PH}C_{PH}/R_{PF}C_{PF}$  coupling at each Motion SPM 2 Product input is recommended in order to prevent input/output signals' oscillation and it should be as close as possible to each of Motion SPM 2 Product pins.

**Fig. 13. Recommended CPU I/O Interface Circuit**

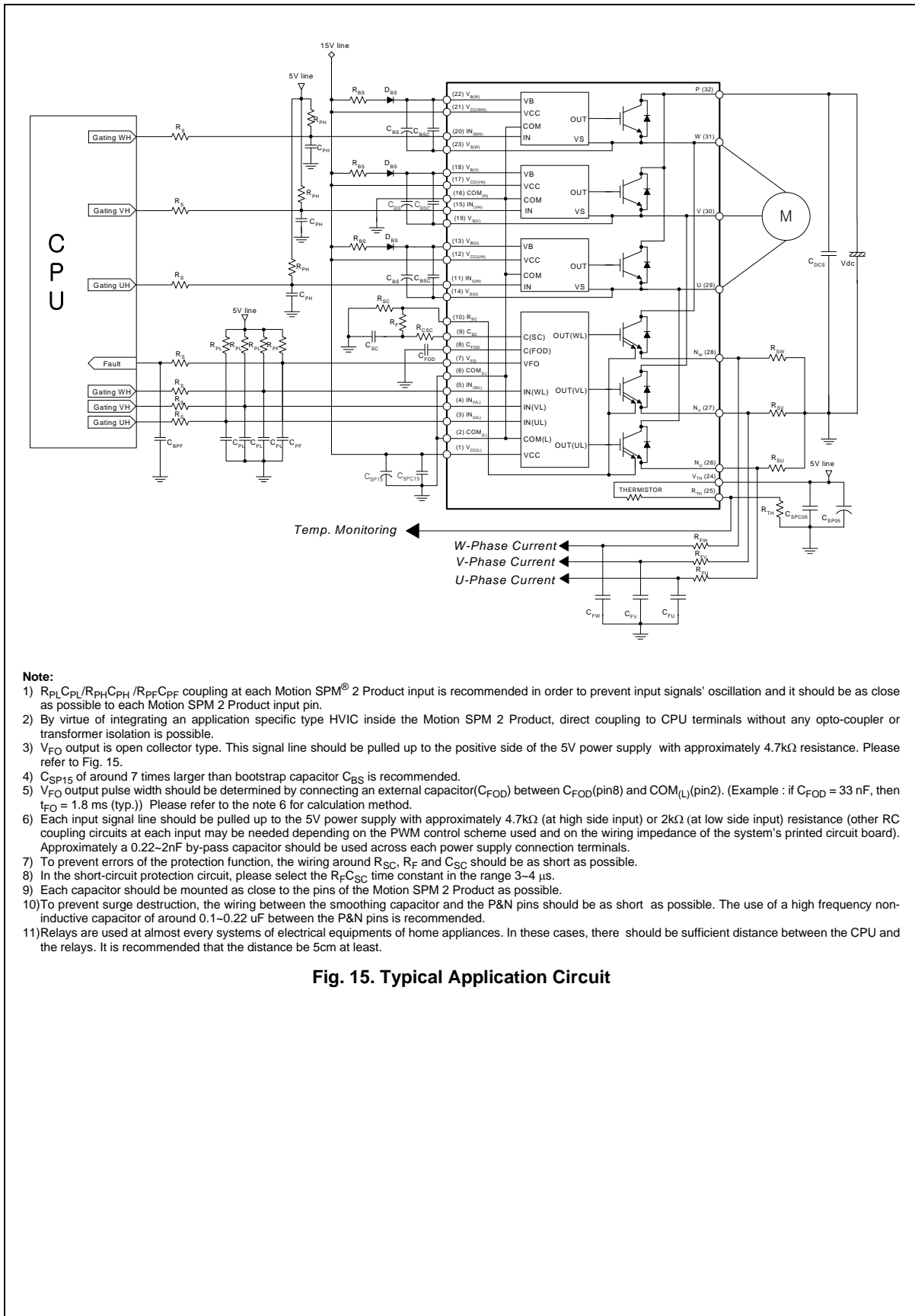
*These Values depend on PWM Control Algorithm*



**Note:**

It would be recommended that the bootstrap diode,  $D_{BS}$ , has soft and fast recovery characteristics.

**Fig. 14. Recommended Bootstrap Operation Circuit and Parameters**



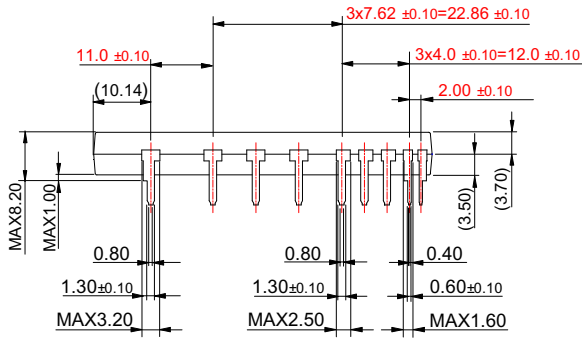
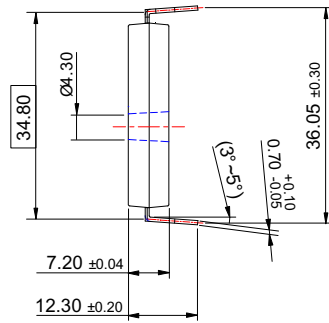
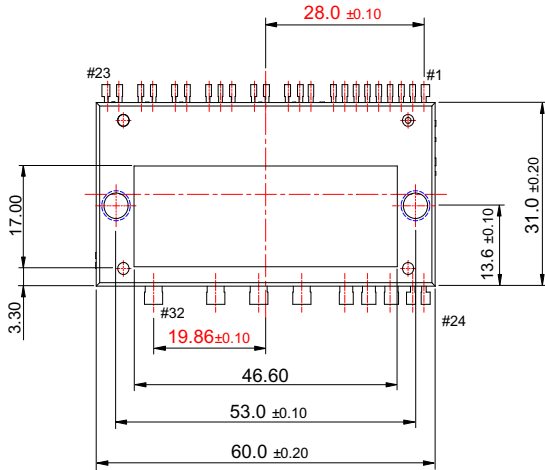
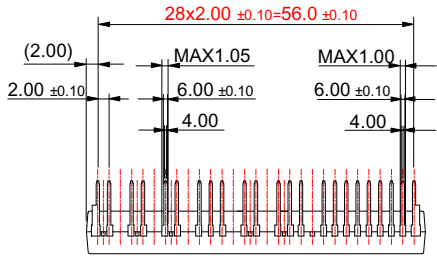
**Note:**

- 1)  $R_{PL}C_{PL}/R_{PH}C_{PH}/R_{PF}C_{PF}$  coupling at each Motion SPM® 2 Product input is recommended in order to prevent input signals' oscillation and it should be as close as possible to each Motion SPM 2 Product input pin.
- 2) By virtue of integrating an application specific type HVIC inside the Motion SPM 2 Product, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.
- 3)  $V_{FO}$  output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 4.7k $\Omega$  resistance. Please refer to Fig. 15.
- 4)  $C_{SP15}$  of around 7 times larger than bootstrap capacitor  $C_{BS}$  is recommended.
- 5)  $V_{FO}$  output pulse width should be determined by connecting an external capacitor( $C_{FOD}$ ) between  $C_{FOD}$ (pin8) and  $COM_{(L)}$ (pin2). (Example : if  $C_{FOD} = 33$  nF, then  $t_{FO} = 1.8$  ms (typ.)) Please refer to the note 6 for calculation method.
- 6) Each input signal line should be pulled up to the 5V power supply with approximately 4.7k $\Omega$  (at high side input) or 2k $\Omega$  (at low side input) resistance (other RC coupling circuits at each input may be needed depending on the PWM control scheme used and on the wiring impedance of the system's printed circuit board). Approximately a 0.22~2nF by-pass capacitor should be used across each power supply connection terminals.
- 7) To prevent errors of the protection function, the wiring around  $R_{SC}$ ,  $R_F$  and  $C_{SC}$  should be as short as possible.
- 8) In the short-circuit protection circuit, please select the  $R_F C_{SC}$  time constant in the range 3~4  $\mu$ s.
- 9) Each capacitor should be mounted as close to the pins of the Motion SPM 2 Product as possible.
- 10) To prevent surge destruction, the wiring between the smoothing capacitor and the P&N pins should be as short as possible. The use of a high frequency non-inductive capacitor of around 0.1~0.22  $\mu$ F between the P&N pins is recommended.
- 11) Relays are used at almost every systems of electrical equipments of home appliances. In these cases, there should be sufficient distance between the CPU and the relays. It is recommended that the distance be 5cm at least.

**Fig. 15. Typical Application Circuit**

Detailed Package Outline Drawings

S32AA-032






Dimensions in Millimeters





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