SPMD150STP

1.5 A stepper motor driver module

Features

- Wide supply voltage range, up to 42 V
- 1.5 A output average working current
- Full/half step and micro-stepping drive capability
- Logic signals TTL/CMOS compatible
- Programmable motor phase current
- Selectable slow/fast current decay
- Non dissipative overcurrent protection
- Remote shutdown
- Thermal shutdown
- Module size: 50.8 x 50.8 x 14.7 mm
- Operating temperature range -40°C to 85 °C

Table 1. Device summary

Order code
SPMD150STP

Description

The SPMD150STP is a highly integrated stepper motor driver module, that allows the user to easily design a complete motor control system for two-phase bipolar stepper motors, interfacing directly the microprocessor to the motor.

The SPMD150STP is an easy-to-use fully integrated answer to motion control issues.

The phase current is chopper controlled, allowing good performances and high speed.

Modules offer an extensive range of protection such as overcurrent and thermal shut-down, that make it “bullet” proof as required in modern motion control systems.

Metallic case allows module to operate without external heat-sink or ventilation; moreover the sealed and molded package offers a complete protection against harsh environments.

Contents

1 Block diagram and pin connection

Figure 1. Block diagram

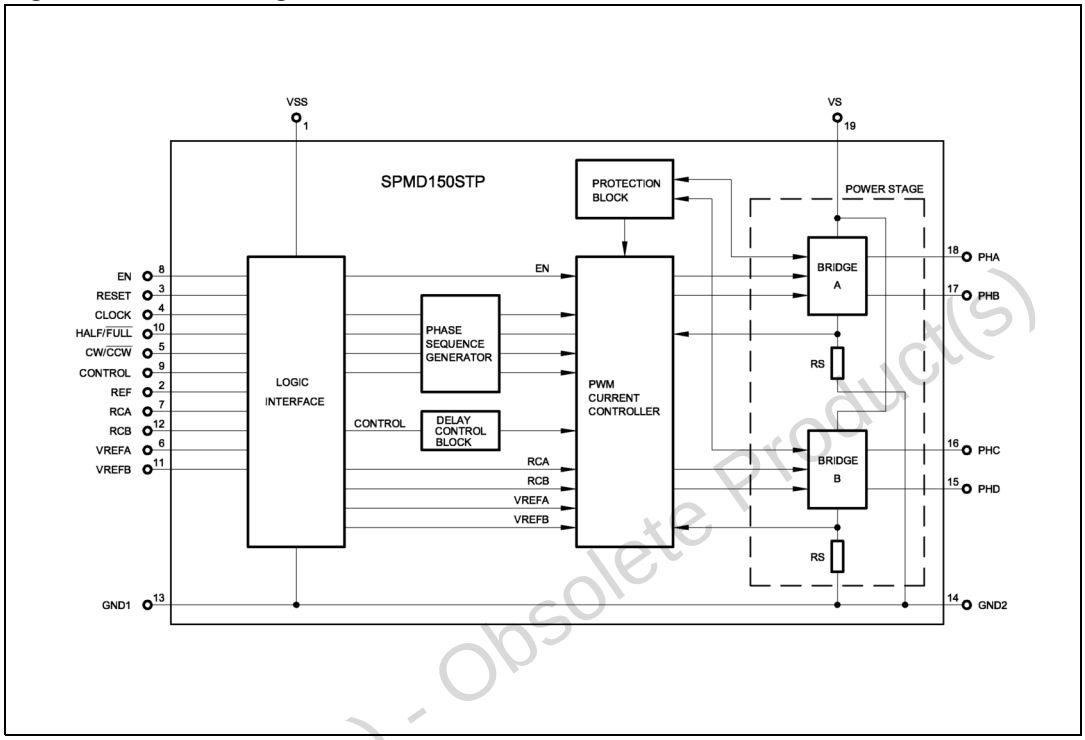


Figure 2. Connection diagram (top view)

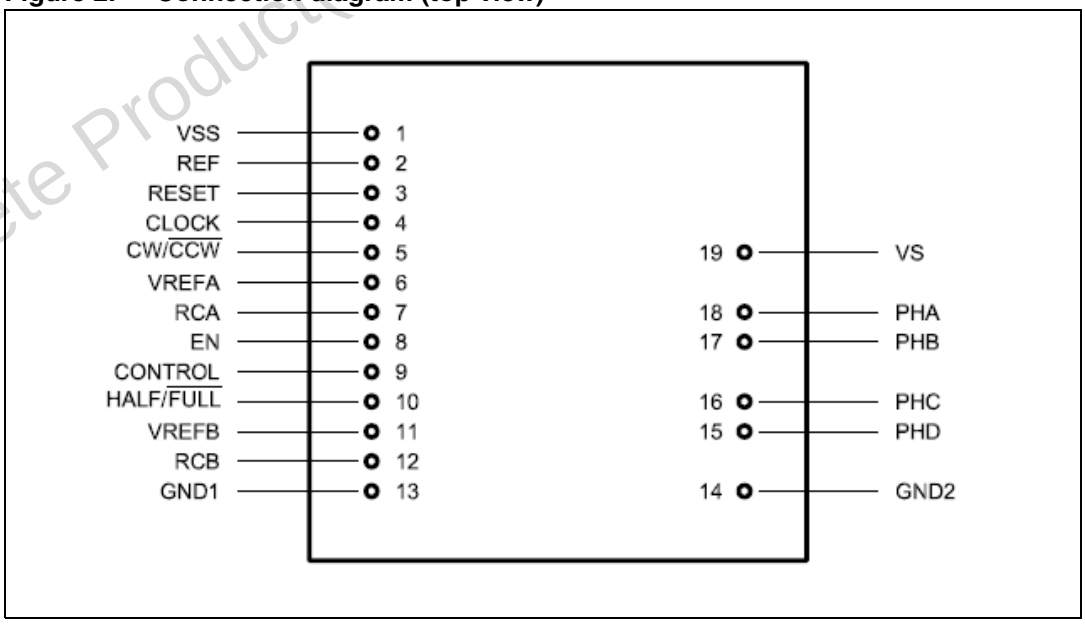


Table 2. Pin description

Pin N.	Name	Function
1	VSS	Logic stage supply voltage. This pin must be supplied with 3.3V or 5V source.
2	REF	Voltage reference output. A voltage of 1.225V is available at this pin. It can be used to set the output current level.
3	RESET	Reset pin. A logic level low restores the home state (State 1) on the phase sequence generator. A 10kΩ pull-up resistor is internally connected to VSS.
4	CLOCK	Step clock. On the rising edge of this signal, the phase sequence generator changes its state position, consequently the motor performs a step. A 10kΩ pull-up resistor is internally connected to VSS.
5	CW/$\overline{CCW}$	Spin direction control input. A logic level high sets clockwise motor rotation. A logic level Low sets counter clockwise motor rotation.Physical direction of rotation depends on windings connection also. A 10 kΩ pull-up resistor is internally connected to VSS.
6	VREFA	Phase A/B current setting input. Connect this pin to a properly scaled REF (Pin2) voltage, to fix the maximum phase output current. Connecting a variable voltage source (i.e. microcontroller DAC), it is possible to perform micro-stepping drive. The pin is internally connected to a 100kΩ pull-down resistor, with a 470pF parallel capacitor.
7	RCA	Phase A/B current controller Off-Time set pin. Use this pin to set the desired Off-time of the switching current controller. A 470pF capacitor and 56kΩ resistor are internally connected between this pin and GND1 (Pin13), giving a 16µs -time.
8	EN	Module enable input. A high logic level enables module operation. EN (pin8) must be low, during power-up and power-down sequence, High during normal operation. (When this input is low, the output phases are in high impedance state, enabling the manual positioning of the motor). A 100kΩ pull-up resistor is internally connected to VSS. A 100nF capacitor is internally connected to GND1
9	CONTROL	Phase current decay mode selection input. A logic level high sets the slow decay mode. A logic level low sets the fast decay mode A 10kΩ pull-up resistor is internally connected to VSS.
10	HALF/$\overline{FULL}$	Half/Full step mode selection input. A logic level high sets the half step mode. A logic level low sets the full step mode. A 10kΩ pull-up resistor is internally connected to VSS.
11	VREFB	Phase C/D current setting input. Connect this pin to a properly scaled REF (Pin2) voltage, to fix the maximum phase output current. Connecting a variable voltage source (i.e. microcontroller DAC), it is possible to perform micro-stepping drive. The pin is internally connected to a 100kΩ pull-down resistor, with a 470pF parallel capacitor.

Table 2. Pin description (continued)

Pin N.	Name	Function
12	RCB	Phase C/D current controller -Time set pin. Use this pin to set the desired Off-time of the switching current controller. A 470pF capacitor and 56kΩ resistor are internally connected between this pin and GND1 (Pin13), giving a 16 µs -time.
13	GND1	Logic stage GND. Return path for the logic signals and VSS (pin1) supply voltage.
14	GND2	Power stage GND. Return path for the power stage and VS (pin19) supply voltage.
15	PHD	Phase D output
16	PHC	Phase C output
17	PHB	Phase B output
18	PHA	Phase A output
19	VS	Power stage supply voltage. Module and motor supply voltage. Maximum voltage must not exceed the specified values.

2 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	DC supply voltage (pin19)	50	V
V_{SS}	DC logic supply voltage (pin1)	7	V
V_{input}	Voltage range at pins VREFA, VREFB, RCA, RCB, EN, CLOCK, CW/$\overline{CCW}$, HALF/$\overline{FULL}$, CONTROL	-0.3 to 7	V
Io-pk	Output peak current	2.5	A
T_{stg}	Storage temperature range	– 40 to +105	°C
T_{op}	Operating case temperature range	– 40 to +85	°C

3 Electrical characteristics

T_A = 25 °C and V_S = 24 V, V_{SS} = 5 V unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
Power stage						
V_S	DC supply voltage		10		42	V
I_S	Quiescent supply current (pin19)	All bridges		5	10	mA
$V_{Sth(ON)}$	Turn-on Input threshold		6.6	7	7.4	V
$V_{Sth(OFF)}$	Turn-off Input threshold		5.6	6	6.4	V
ΔV_{VS-PH}	Output voltage drop (VS to pins 15,16,17,18)	Io = -1.5A			0.9	V
ΔV_{PH-GND}	Output voltage drop (Pins15,16,17,18 to GND2)	Io = 1.5A			1.1	V
Io	Phase average working current				±1.5	A
Protections block						
Io-sc	Phase short circuit current	Internally limited by overcurrent protection (*Figure 7*)	4	5.6	7.1	A
$t_{OCD(ON)}$	Overcurrent detection turn-on delay time	(*Figure 7*)	200			ns
$t_{OCD(OFF)}$	Overcurrent detection turn-off delay time	(*Figure 7*)	100			ns
$T_{j(OFF)}$	Junction shutdown temperature			165		°C
Logic interface						
V_{SS}	DC logic supply voltage		3.0	5	5.25	V
I_{SS}	Quiescent supply current (pin 1)	All inputs open			1.2	mA
V_{IL}	Low level input voltage	Pin 5,9,10 V_{SS} = 3 to 5.25V	-0.3		0.8	V
V_{IH}	High level input voltage	Pin 5,9,10 V_{SS}=3 to 5.25V	2		Vss	V
Vth(ON)	Turn-on input threshold	Pin 3,4,8 V_{SS}=3 to 5.25V (*Figure 1*, *2*, *3*, *4*)		1.8	2.0	V
Vth(OFF)	Turn-off input threshold	Pin 3,4,8 V_{SS}=3 to 5.25V (*Figure 1*, *2*, *3*, *4*)	0.8	1.3		V
Vth(HYS)	Input threshold hysteresis	Pin 3,4,8 V_{SS}=3 to 5.25V (*Figure 1*, *2*, *3*, *4*)	0.25	0.5		V
I_{IL}	Low level Input current	Pin 3,4,5,8,9,10		-0.5		mA

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Value			Unit
			Min	Typ	Max	
I_{IH}	High level Input current	Pin 3,4,5,8,9,10		10		uA
V_{REF}	Reference output voltage (pin 2)		1.21	1.225	1.24	V
REF_res	Reference output resistance (pin2)			10		kΩ
VREFx_res	Current setting input resistance (pin 6,11)			100		kΩ
Timing definition						
$t_{D(ON)EN}$	Enable to output turn-on delay	Io=2.5A, resistive load (*Figure 3*)	100	250	400	ns
$t_{D(OFF)EN}$	Enable to output turn-off delay	Io=2.5A, resistive load (*Figure 3*)	300	550	800	ns
t_{RISE}	Output rise time	Io=2.5A, resistive load (*Figure 3*)	40		250	ns
t_{FALL}	Output fall time	Io=2.5A, resistive load (*Figure 3*)	40		250	ns
t_{DCLK}	Clock to output delay time	Io=2.5A, resistive load (*Figure 4*)		2		µs
$t_{CLK(MIN)L}$	Clock minimum low level time	(*Figure 5*)			1	µs
$t_{CLK(MIN)H}$	Clock minimum high level time	(*Figure 5*)			1	µs
f_{CLK}	Clock frequency				50	kHz
$t_{S(MIN)}$	Minimum set-up time	(*Figure 6*)			1	µs
$t_{H(MIN)}$	Minimum hold time	(*Figure 6*)			1	µs
$t_{R(MIN)}$	Minimum reset time	(*Figure 6*)			1	µs
$t_{RCLK(MIN)}$	Minimum reset to clock delay time	(*Figure 6*)			1	µs

Figure 3. Switching characteristic definition

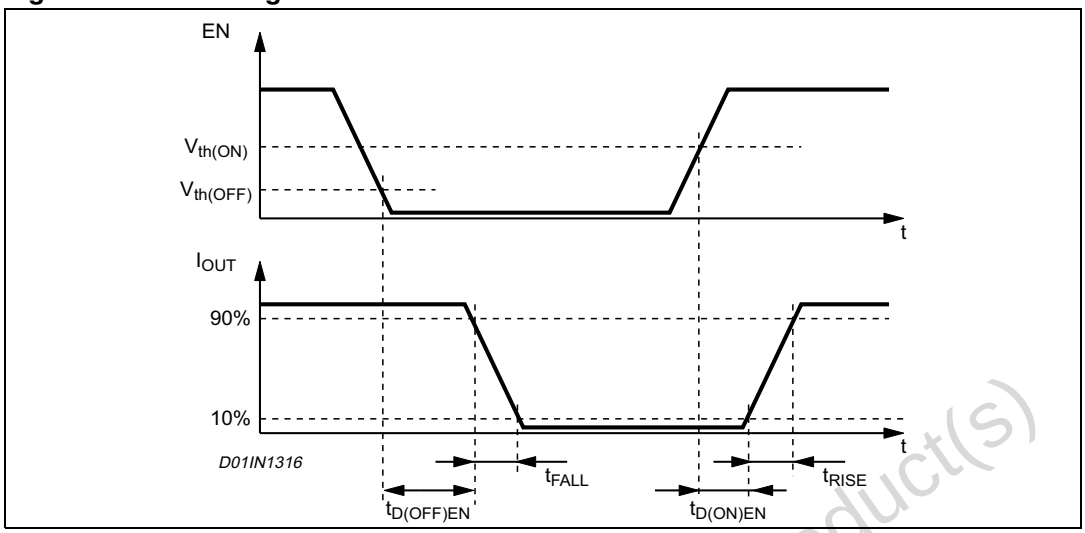


Figure 4. Clock to output delay time

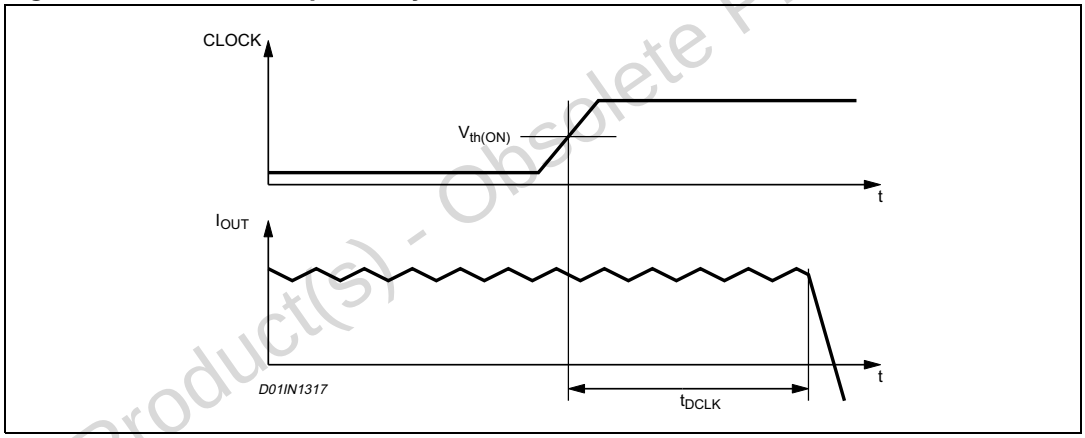


Figure 5. Minimum timing definition: clock

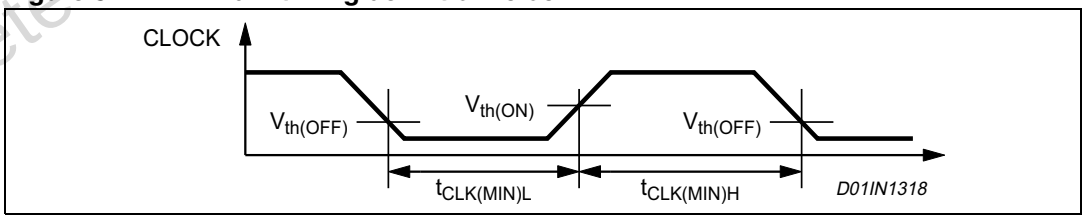


Figure 6. Minimum timing definition: logic inputs

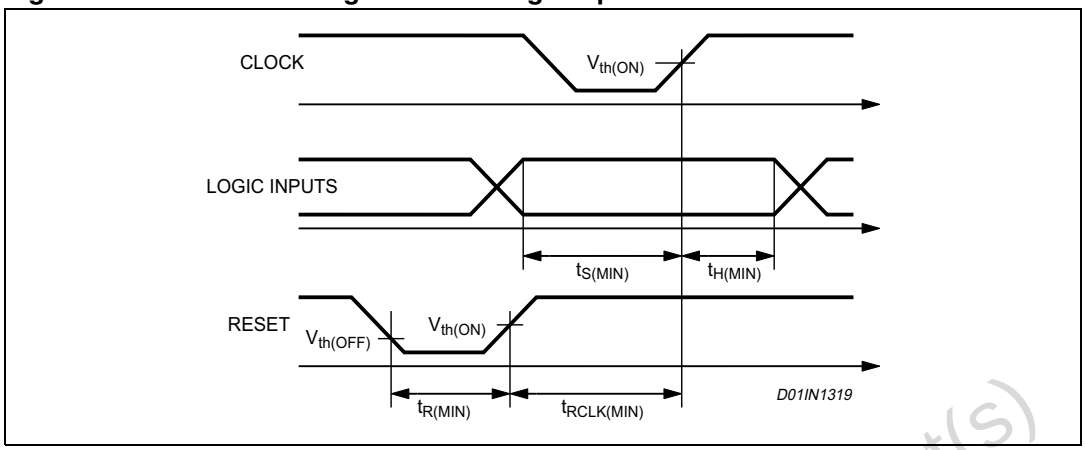
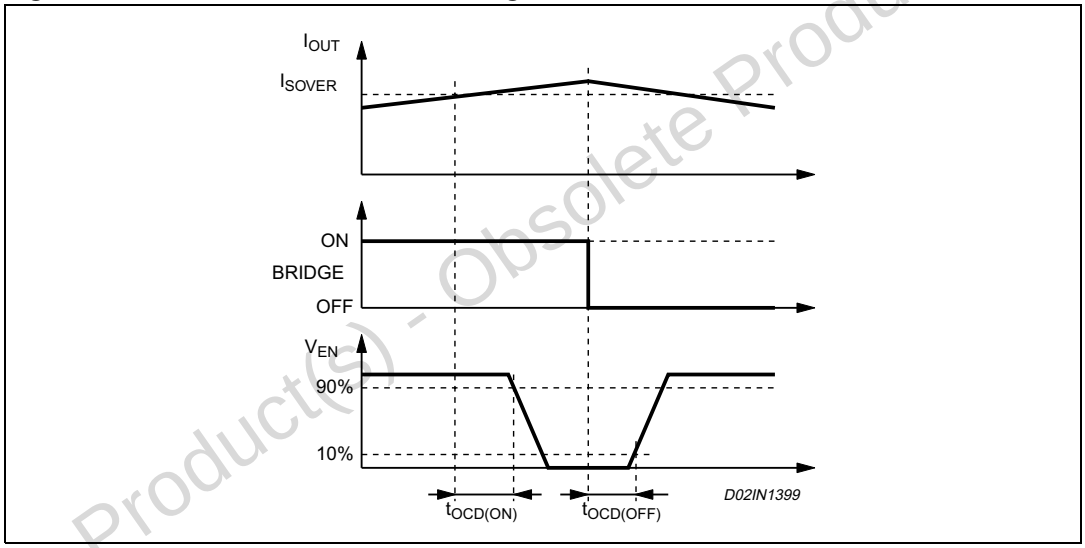


Figure 7. Overcurrent detection timing definition



4 Function description and application information

SPMD150STP can be seen divided in several main blocks (see *Figure 1*):

- Power stage, to drive the motor windings
- Logic interface, to interface the external signals to the internal circuitry
- PWM current controller, to fix and control the current flowing in the motor phase windings
- Decay control block, to control the phase current decay mode
- Phase sequence generator, to generate the motor phases driving sequence
- Protection block, performing over current protectionand thermal shut-down to protect the power bridges

4.1 Power stage

STMD150STP integrates two independent MOSFET full bridges, with intrinsic fast freewheeling diodes. Switching patterns are generated by the phase sequence generator and by the PWM current controller.

The power MOSFET cross conduction in one bridge leg, is avoided introducing a dead time (t_{DT} = 1 µs typical), between FETs switch off and the switch on.

VS (pin19) and GND2 (pin14) must be connected to the supply voltage, which can range from 10 V to 42 V.

4.2 Logic interface

Logic interface connects the external logic signal to the proper internal blocks.

RESET (pin3), CLOCK (pin4), CW/$\overline{\text{CCW}}$ (pin5), CONTROL (pin9) and HALF/$\overline{\text{FULL}}$ (pin10) have a 10kΩ pull-up resistor to VSS (pin1), in order to prevent floating pins;

VSS can be connected to 3.3 V or 5 V, allowing the interface with the most popular microcontroller. The internal structure is shown in *Figure 8*.

EN (pin8) has identical input structure, with the exception that the MOSFET drain of the over-current and thermal protection is also connected to this pin (see *Figure 9*).

Due to this connection some care needs to be taken in driving this pin.

Inside the module a 100 kΩ resistor and a 100 nF capacitor is provided, an open collector driving is therefore the suggested solution.

Figure 8. Logic inputs internal structure

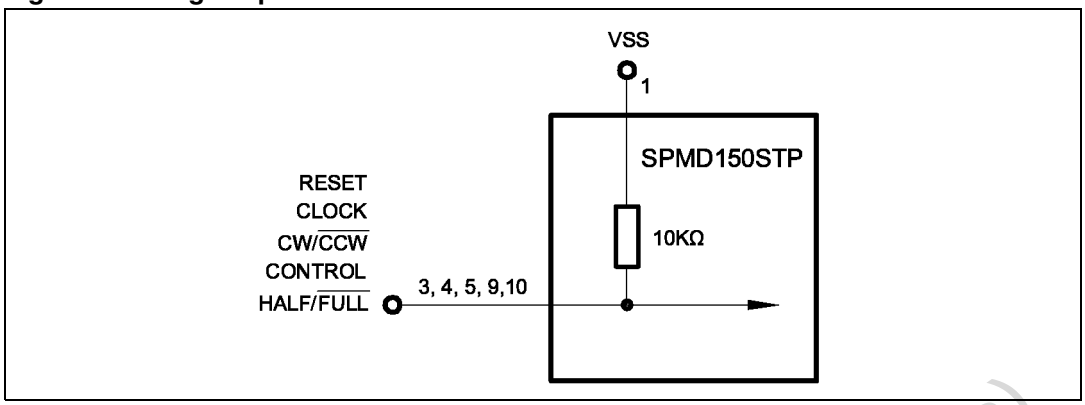
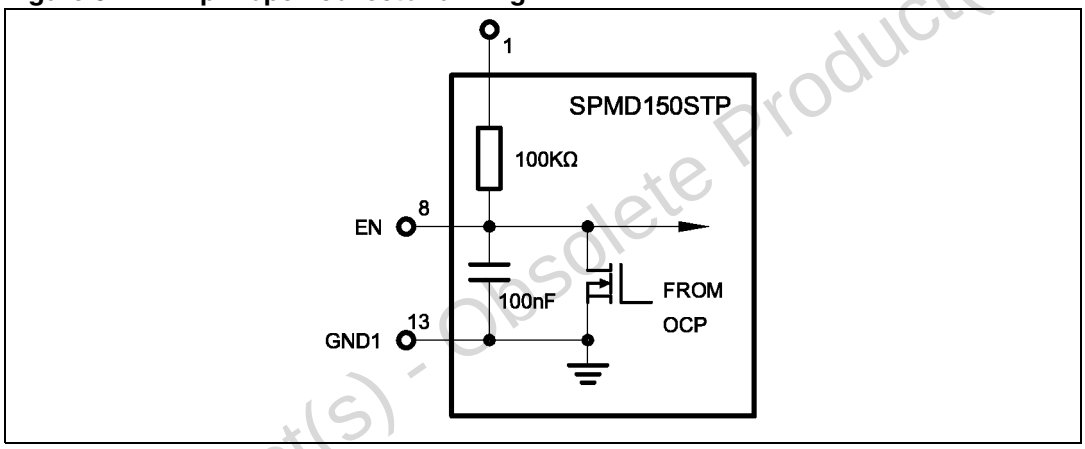


Figure 9. EN pin open collector driving



4.3 PWM current controller

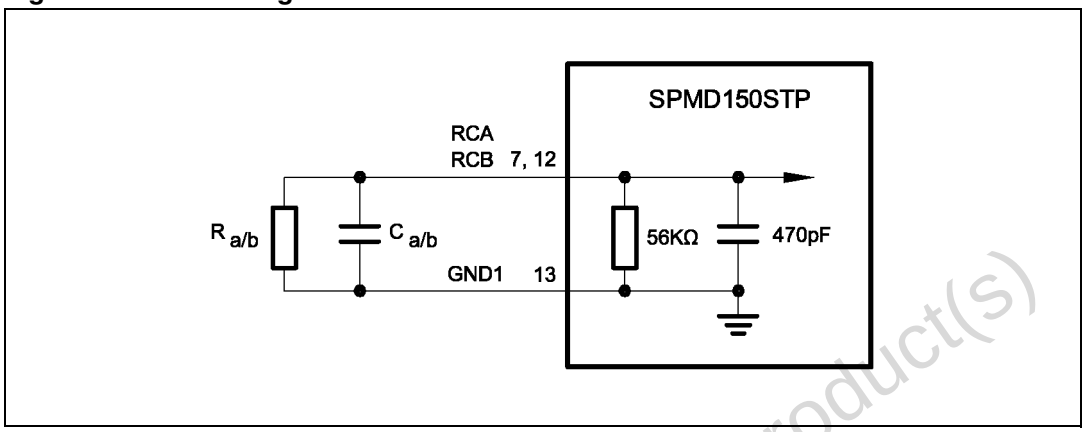
The control block is composed by a constant Off-time PWM current controller for both two bridges. The current control circuit senses the bridge current, by sensing the voltage drop across a sense resistor connected between the source of the two lower power MOSFETs and ground. As the current in the motor buildup, the voltage across the sense resistor increases proportionally. When the voltage on the sense resistor becomes greater than the voltage at the reference inputs VREFA (pin6) or VREFB (pin11), the sense comparator triggers a mono-stable circuit, switching the bridge off.

The bridge MOSFETs remain off for the time set by pin RCA (pin7) or RCB (pin12);

during this Off-time (see *Figure 11*, toff versus Roff and Coff), the motor phase current re-circulates as defined by the selected decay mode, described in the next section. When the mono-stable circuit times out, the bridge will turn on again. Since the internal dead time t_{DT}, used to prevent cross conduction in the bridge, delays the turn on of the power MOSFETs, the effective Off-time is the sum of the mono-stable time plus the t_{DT} (1µs). To set the toff relative to Bridge A, it is necessary to connect a proper resistor Ra and/or a proper capacitor Ca in parallel between pin RCA and GND1, see *Figure 10* and *Figure 11*; To set the toff relative to Bridge B, it is necessary to connect a proper resistor Rb and/or a proper capacitor Cb in parallel between pin RCB and GND1, see *Figure 10* and *Figure 11*; A 56 kΩ resistor and a 470 pF capacitor are already present between pin RCA/B and GND1 inside the

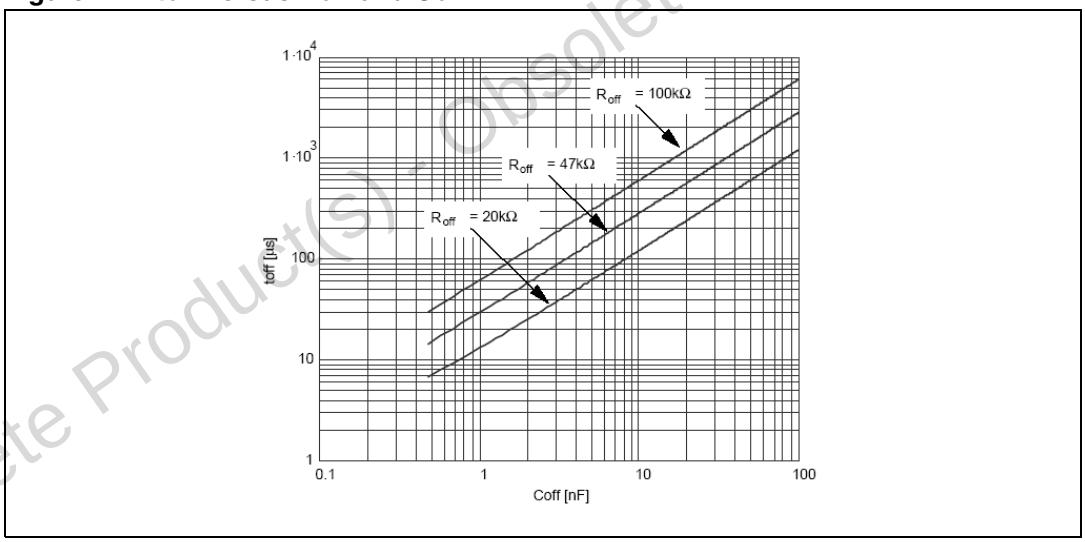
module, fixing a typical 16 µs off time for both bridges. The toff value can be modified adding a capacitor to GND1, increasing the off time, or adding a resistor to GND1 decreasing the Off-time.

Figure 10. toff setting circuit



Roff = Ra // 56kΩ [kΩ], Coff = Ca + 470pF [pF]

Figure 11. toff versus Roff and Coff



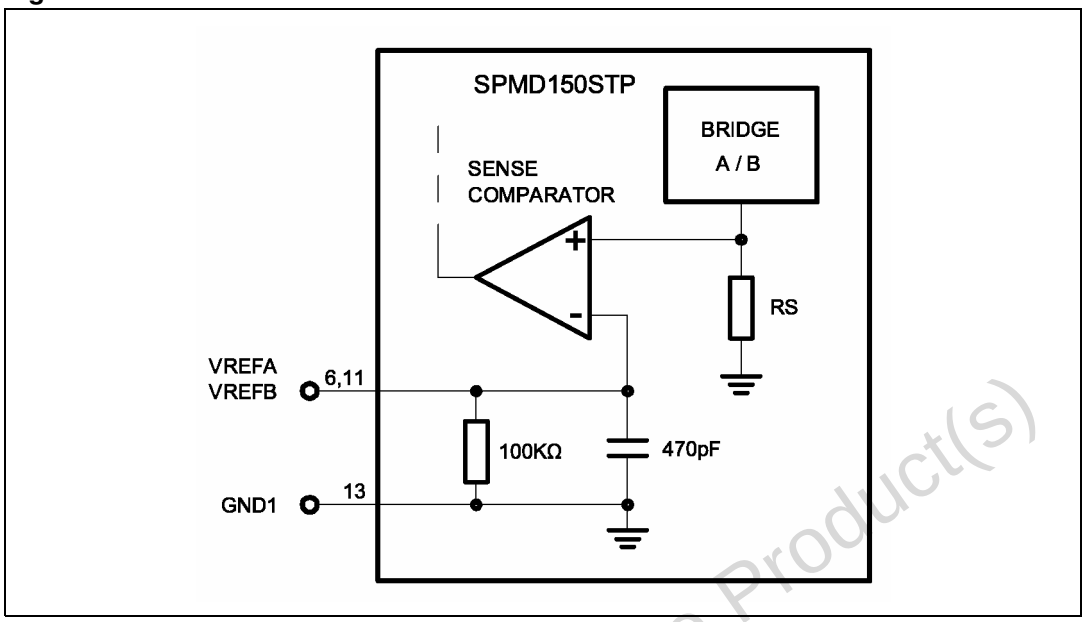
To set the maximum motor phase current it is necessary to give the proper reference voltage at input VREFA (pin6) and VREFB (pin11).

The relationship between the voltage at VREFx pin and the phase current I_{OUTx} is the following:

I_{OUTx} = VREFx / 0.192 [A]

An internal 100 kΩ resistor and a 470 pF capacitor are connected in parallel between VREFx and GND1 (see *Figure 12*).

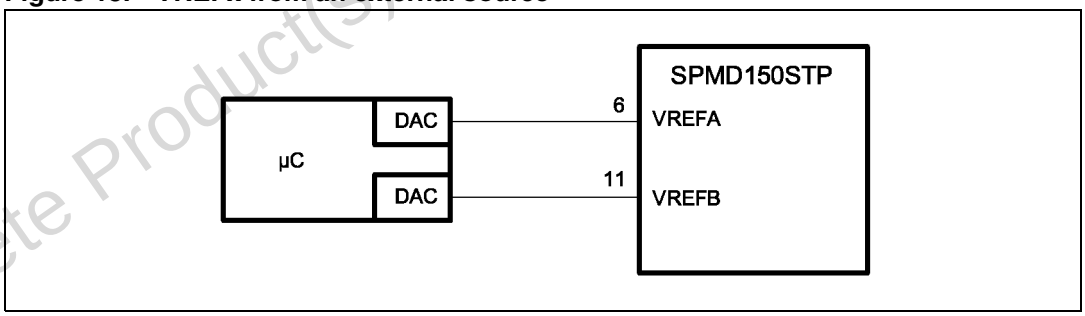
Figure 12. VREFA and VREFB internal connection



The voltage at VREFA and VREFB can be supplied in two way:

- Using an external source (see *Figure 13*), driving VREFA and VREFB pins together or separately as in the micro-stepping mode (i.e: a micro-controller fixes a variable voltage to get variable current in the stepper motor phases).

Figure 13. VREFx from an external source

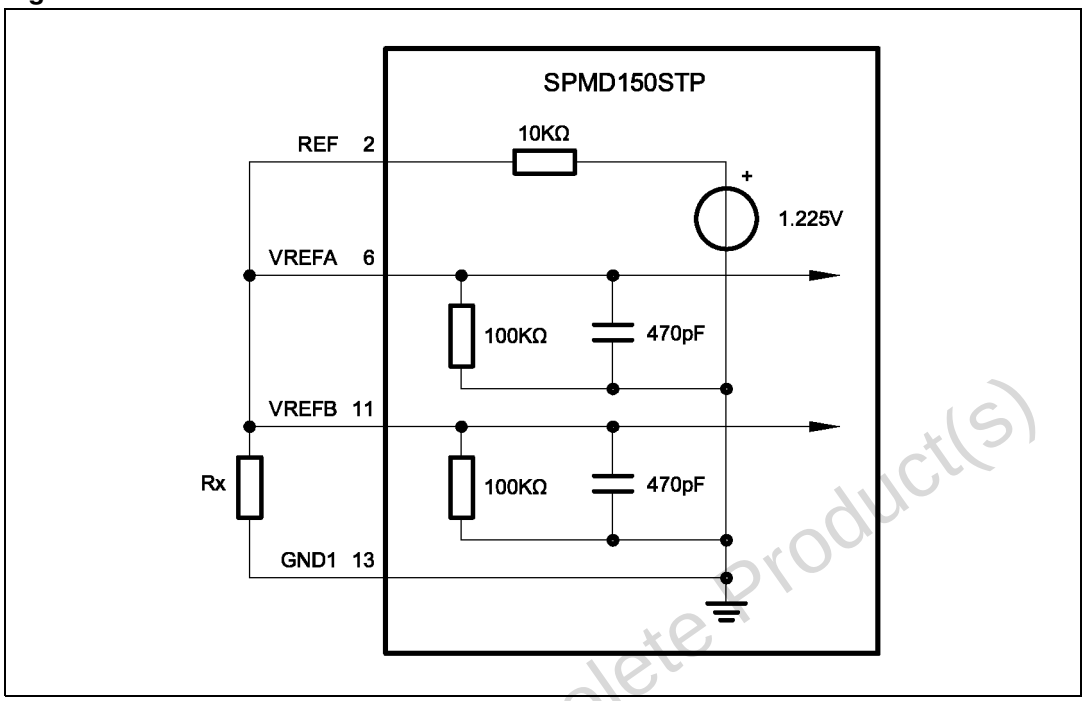


- Using the module reference voltage source, REF (pin2) (see *Figure 14*), which supplies 1.225 V. The REF pin has a 10 kΩ resistor in series, take that in account during design.
- In this case a proper resistor Rx must be connected between REF and GND1, VREFA and VREFB will be connected together to REF pin (see *Figure 14*).

Use following equation to calculate Rx:

$$Rx = (500 \times I_{OUTx}) / [319 - (60 \times I_{OUTx})] \quad [k\Omega] \qquad \text{where } I_{OUTx} = [A]$$

Figure 14. VREFx from internal source



4.4 Decay modes

The CONTROL input is used to select the behavior of the bridge during the off time. When the CONTROL pin is low, the fast decay mode is selected and both transistors in the bridge are switched off during the off time.

When the CONTROL pin is high, the slow decay mode is selected and only the low side transistor of the bridge is switched off during the off time.

Figure 15 shows the operation of the bridge in the fast decay mode. At the start of the off time, both of the power MOSFETs are switched off and the current recirculates through the two opposite free wheeling diodes. The current decays with a high di/dt, since the voltage across the coil is essentially the power supply voltage. After the dead time, the lower power MOSFET in parallel with the conducting diode is turned on in synchronous rectification mode. In applications where the motor current is low it is possible that the current can decay completely to zero during the off time. At this point if both of the power MOS were operating in the synchronous rectification mode it would then be possible for the current to build in the opposite direction. To prevent this only the lower power MOS is operated in synchronous rectification mode. This operation is called quasi-synchronous rectification mode. When the mono-stable circuit times out, the power FETs are turned on again after some delay set by the dead time to prevent cross conduction.

Figure 15. Fast decay mode output stage configurations

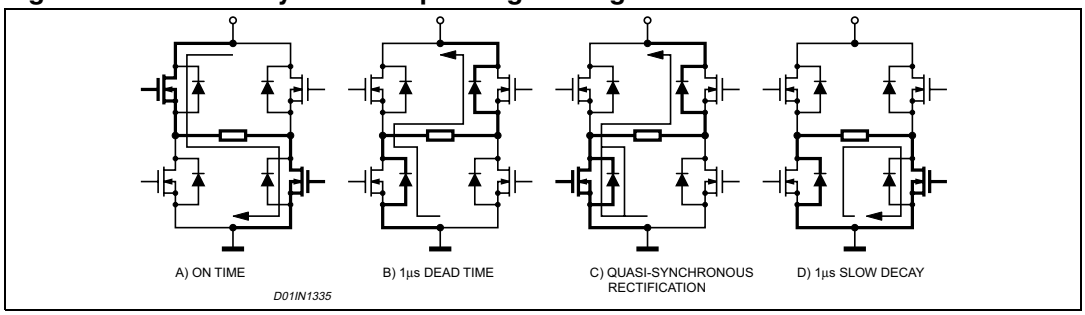
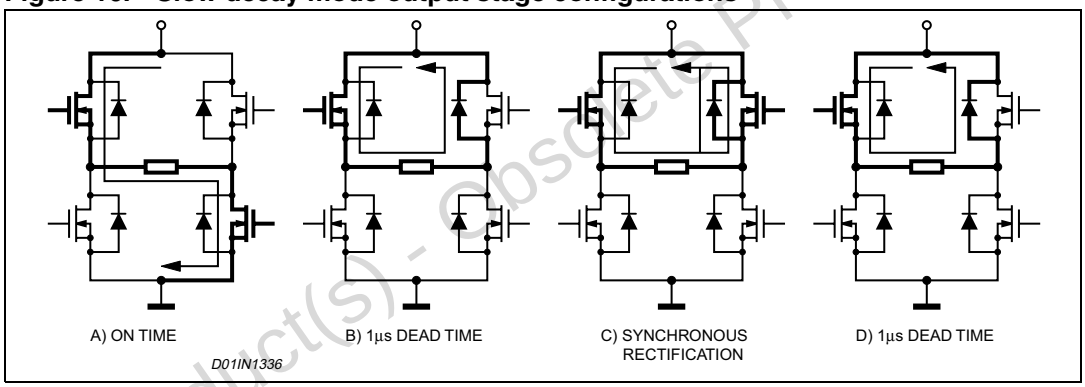


Figure 16 shows the operation of the bridge in the slow decay mode. At the start of the Off-time, the lower power FET is switched off and the current recirculates around the upper half of the bridge. Since the voltage across the coil is low, the current decays slowly. After the dead time the upper power FET is operated in the synchronous rectification mode. When the mono-stable circuit times out, the lower power FET is turned on again after some delay set by the dead time to prevent cross conduction.

Figure 16. Slow decay mode output stage configurations



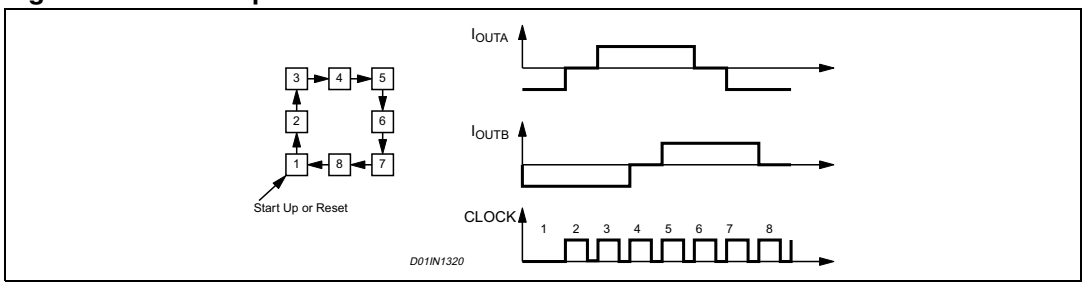
4.5 Stepping sequence generation

The phase sequence generator is a state machine that provides the phase and the enable inputs for the two bridges to drive a stepper motor in either full step or half step. Two full step modes are possible, the normal drive mode where both phases are energized each step and the wave drive mode where only one phase is energized at a time. The drive mode is selected by the HALF/$\overline{\text{FULL}}$ input and the current state of the sequence generator as described below. A rising edge of the CLOCK input advances the state machine to the next state. The direction of rotation is set by the CW/$\overline{\text{CCW}}$ input. The RESET input resets the state machine to Home State.

4.5.1 Half step mode

A logic level high on the HALF/$\overline{\text{FULL}}$ input selects half step mode. *Figure 17* shows the motor current waveforms and the state diagram for the phase sequencer generator. At start-up or after a RESET the phase sequencer is at state 1, home state. After each clock pulse the state changes following the sequence 1,2,3,4,5,6,7,8,… if CW/ $\overline{\text{CCW}}$ is high (Clockwise movement) or 1,8,7,6,5,4,3,2,… if CW/$\overline{\text{CCW}}$ is low (Counterclockwise movement).

Figure 17. Half step mode



4.5.2 Normal drive mode (full-step two-phase-on)

A Low level on the HALF/$\overline{\text{FULL}}$ input selects the full step mode.

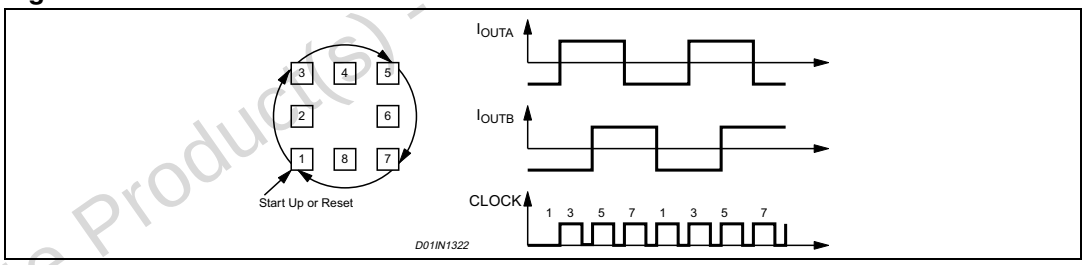
If the low level is applied when the state ma1chine is at an ODD numbered state, the normal drive mode is selected.

Figure 18 shows the motor current waveform state diagram for the state machine of the phase sequencer generator.

The normal drive mode can be selected easily, by holding the HALF/$\overline{\text{FULL}}$ input low and applying a RESET. AT start -up or after a RESET the state machine is in state1.

After the HALF/$\overline{\text{FULL}}$ input is kept low, state changes following the sequence 1,3,5,7,… if CW/$\overline{\text{CCW}}$ is high (Clockwise movement) or 1,7,5,3,… if CW/CCW is low (Counterclockwise movement).

Figure 18. Normal drive mode



4.5.3 Wave drive mode (full-step one-phase-on)

A low level on the pin HALF/$\overline{\text{FULL}}$ input selects the full step mode.

If the low level is applied when the state machine is at an EVEN numbered state, the wave drive mode is selected.

Figure 19 shows the motor current waveform and the state diagram for the state machine of the phase sequence generator.

To enter the wave drive mode the state machine must be in an EVEN numbered state.

An example of selecting the wave drive mode is the following:

to apply a RESET first;

keeping the HALF/$\overline{\text{FULL}}$ input high, to apply one pulse to the CLOCK input;

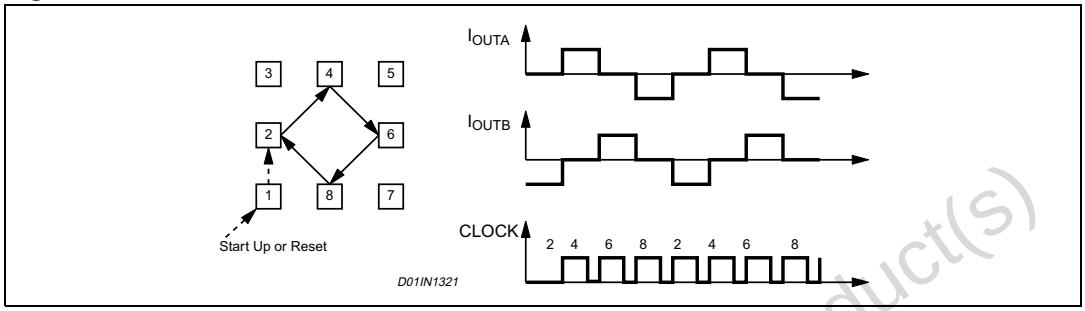
then, to apply the logic level Low to the HALF/$\overline{\text{FULL}}$ input.

This sequence first forces the state machine to sate 1.

The clock pulse, with the HALF/$\overline{\text{FULL}}$ input high, advances the state machine from state 1 to either state 2 or 8 depending on the CW/$\overline{\text{CCW}}$ input.

Starting from this point, keeping the HALF/$\overline{\text{FULL}}$ input low, the state machine will advance following the sequence 2,4,6,8,… if CW/$\overline{\text{CCW}}$ is high (Clockwise movement) or 8,6,4,2,… if CW/ $\overline{\text{CCW}}$ is low (Counterclockwise movement).

Figure 19. Wave drive mode



4.5.4 Microstepping

STMD150STP has two separate control current loop, with the possibility to set the current level in an independent way (by means VREFA and VREFB); this feature make possible the actuation of the micro-stepping mode.

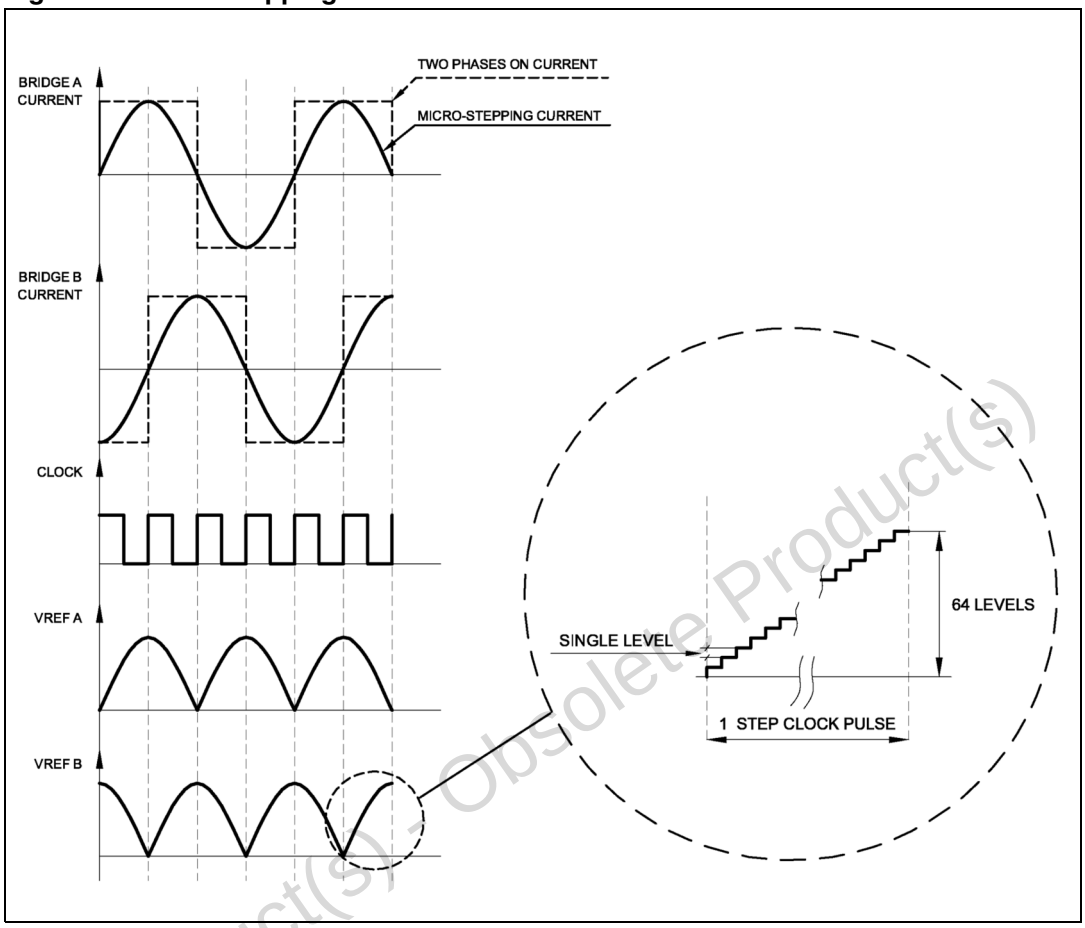
Micro-stepping mode is a full step mode performed with a not fixed current in the motor phases, but with a current varying in a sinusoidal mode;

that means the current flowing in the motor is not a square wave, but a sinusoidal wave.

Main commands remain the same, but during the period of each clock step, VREFA and VREFB are incremented or decremented through a defined number of level, this number gives the name to the micro-stepping granularity;

as example, a 64 micro-step per step means that, for each “standard” step there are 64 step values on VREFA/B (from zero to VREFA/B max and from VREFB/A max to zero, see *Figure 20*)

Figure 20. Microstepping



4.6 Non-dissipative overcurrent protection

The SPMD150STP integrates an overcurrent protection circuit.

This circuit provides protection against a short circuit to ground or between two phases of the bridge.

To implement the over current detection, a sensing element that delivers a small but precise fraction of the output current is implemented with each high side power MOSFET.

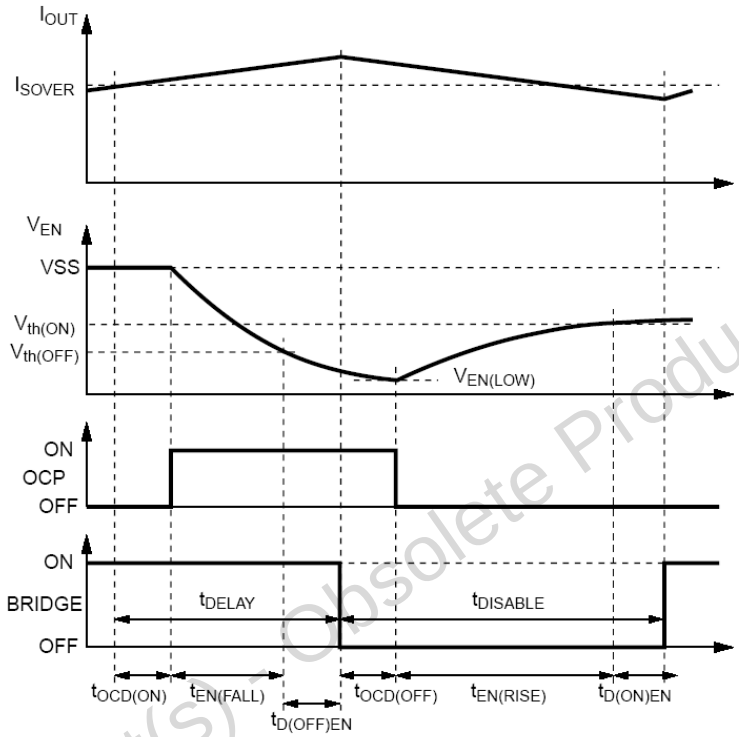
Since this current is a small fraction of the output current, there is very little additional power dissipation.

This current is compared with an internal reference, when the output current reaches the detection threshold (typically 5.6A) the OCP comparator signals a fault condition.

If a fault condition is detected, the EN pin is pulled below the turn off threshold (1.3V typical) by an internal open drain MOSFET with a pull down capability of 4mA.

An internal100 kΩ resistor plus a 100 nF capacitor connected to the EN pin, seta 400 µs off time, before recovering normal operation (see *Figure 9* and *Figure 21*).

Figure 21. Overcurrent protection waveforms



4.7 Thermal characteristics

The case-to-ambient thermal resistance is 8 °C/W. This produces a 40 °C temperature increase of the module surface for 5 W of internal dissipation.

According to ambient temperature and/or to maximum case operating temperature (85 °C), an additional heat sink or forced ventilation may be required.

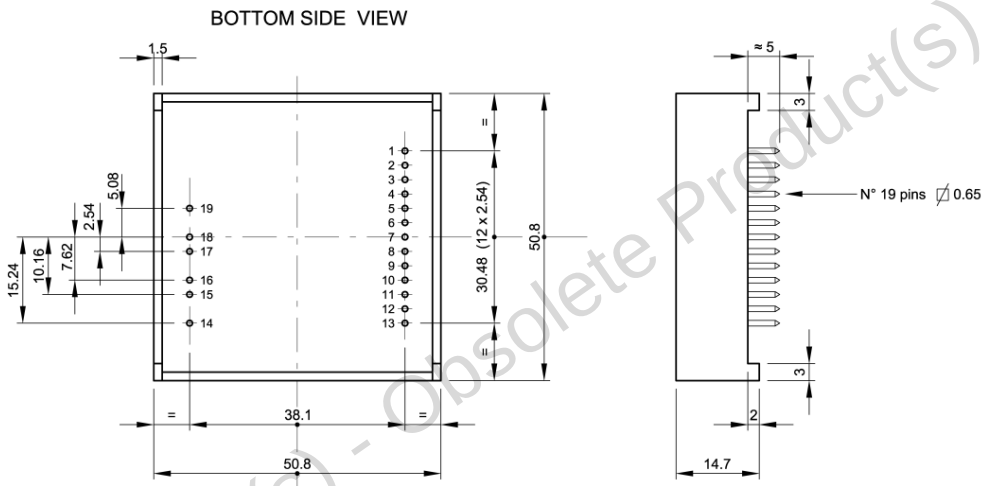
4.8 Case grounding

The module case is internally connected to GND1 (pin13) and GND2 (pin14). To obtain additional effective EMI shield, the PCB area below the module can be used as an effective sixth side shield.

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 22. Package dimensions



6 Revision history

Table 5. Document revision history

Date	Revision	Changes
22-Feb-2010	1	First release

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